IMPROVED TRANSIENT STABILITY AND POWER TRANSFER DURING SINGLE POLE SWITCHING: A SYMMETRICAL SEQUENCE FILTERING APPROACH

by

ORLANDO A. CINIGLIO

A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

1991

To my wife

Amalia

TABLE OF CONTENTS

Abstract of Dissertation Presented to the Graduate School of the University of Florida in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy

IMPROVED TRANSIENT STABILITY AND POWER TRANSFER DURING SINGLE POLE SWITCHING
A SYMMETRICAL SEQUENCE FILTERING APPROACH

By

Orlando Antonio Ciniglio Manzzo

May 1991

Chairman: Dr. Dennis P. Carroll
Major Department: Electrical Engineering

An innovative compensation scheme which allows three-phase AC transmission lines to be operated with one phase open, on a permanent basis, has been developed. At present, the only times high voltage lines are operated with an open pole, in a controlled mode, is during the dead time of a single pole reclosing operation; usually, not more than a few seconds in duration. The detrimental effects associated with the high levels of negative and zero sequence currents, generated during the single pole opening condition (SPO), preclude permanent operation of the line in two phases.

The concept of selective sequence compensation is hereby introduced. This scheme, also referred to as selective sequence filtering, is a new compensation strategy whereby undesired line sequence current components are confined to flow in a restricted region of the system.

The proposed compensator presents a low impedance path to the flow of selected sequence components of the current. The basic element of this filtering apparatus is composed of an unbalanced reactive compensator, made up of passive elements connected in a general arrangement. Placing our selective sequence compensator at each end of the affected circuit will force the unbalanced currents, produced during the SPO, to circulate within the compensators and the affected line. In this manner, the harmful effects associated with negative and zero sequence currents flowing into the remote systems are eliminated.

A Fortran program was written to compute the required compensation parameters for a typical 500 kv system. Sensitivity studies were carried out to determine the dependency of the various compensator elements on different system operating conditions. The results obtained for the steady state solution were in accordance with the stated goals of this research.

The Electromagnetics Transient Program (E.M.T.P) has been used to evaluate the transient response of the system to selective sequence compensation. The results of the simulation indicate that the operational constraints of the system are not violated during the application of the proposed compensation.

This novel approach will produce improved transient stability margins, for single line to ground type contingencies. The proposed compensation will also provide the means for a more efficient conductor and circuit utilization in a three phase AC system.

CHAPTER 1
INTRODUCTION

This research is aimed at determining a new scheme or strategy that will allow three-phase AC transmission lines to be operated on a permanent basis, with one phase open.
At present, the nearest a high voltage line comes to operate with an open pole, in a controlled mode, is during the dead time of a single pole reclosing sequence, usually not more than one second in duration.

Most of the work done on single pole switching deals mainly with various aspects of the secondary arc current phenomenon. In a single pole reclosure operation, the secondary arc current is that residual current that flows through the primary fault current path, after the associated poles of the faulted phase have opened. Secondary arc current is fed through the capacitive and electromagnetic coupling of the faulted phase with the remaining sound phases.
A successful single pole reclosure operation requires secondary arc current extinction prior to attempting reenergization of the previously faulted conductor.
Kimbark [1] established the basic principles of secondary arc extinction by means of shunted reactor compensation, quenching

out the secondary arc current, by effectively inserting a high impedance in its path, via parallel resonance of the compensating reactor and the interphase capacitances of the line. Shperling et al. [2,3] devised a modified reactor compensation scheme to deal with secondary arc current extinction for untransposed EHV (extra high voltage) lines, providing, through a switchable arrangement of reactors, different degrees of compensation according to the varying requirements of the faulted phase. More recently, Hasibar et al. [4] described the application of high speed grounding switches for single pole reclosing on EHV systems as a means of extinguishing the secondary arc. In their scheme, the recovery voltage across the arc path is reduced to such a value that the flow of secondary arc current will not be sustained.

A large percentage of the high voltage line faults are of the phase to ground type, and most of these are temporary in nature; that is, if momentarily interrupted they will not recur. Single pole switching is a controlled sequence operation by which the pole corresponding to the faulted phase of the line end circuit breakers is open momentarily and then reclosed. If the fault should re-strike within a certain time interval (reset time, generally depends on electric utility operations policy), the controlled switching logic will

immediately send a definite three phase trip to each circuit breaker.

Even though unscheduled high voltage line removals are not common occurrences they are, in general, considered severe events, and, depending on their relative power transfer at the moment of interruption, can lead to an emergency state of the system. An undefinite single pole trip under unsuccessful single pole reclosing operation is considered unacceptable. The unbalances generated during the open pole mode in a short time could overheat and eventually damage motors and generators, produce undesired trips of contiguous lines, increase system losses, create interferences in communication circuits, etc. Even when the reclosing sequence is successful, there is a reduction in power transfer capacity through the line, during the opening cycle, hence affecting the system transient stability limit.

Efforts to diminish the effects of power transfer capacity reduction during the opening cycle of a single phase reclosure sequence have been limited to series capacitor compensation of either the faulted line or the remaining healthy phases. Although theoretically realizable, this scheme is generally not practical due to the large amount of compensation required and other undesired commplications. In those cases where implementation is possible, the unbalanced currents generated during this condition (one pole open) will

restrict the time during which compensation is allowed. Thus, for permanent single phase faults, a definite three phase trip of the line will still be mandatory.

Shipley et al. [5] have performed some simulation studies for determining the effect of grounding the sending end transformer in a radial system through a capacitor as a means of automatically compensating for the power reduction through the line during the opening condition. Even though conceptually simple and straightforward, resultant overvoltages rendered the scheme ineffective.

We have previously investigated the possibility of automatic zero sequence compensation as a means of reducing power transfer capacity during the limiting open pole condition and of simultaneously reducing the unbalance currents to a level that would have allowed for permanent operation in two phases. The complexity of the scheme devised did not appear justifiable.

The present approach is built upon a newly developed method of analysis of system unbalances and the introduction of the concept of resonant symmetrical sequence filter and its implementation. An ungrounded network is initially considered and the compensation proven effective. Consequently, the concept has been extended to cover the more common grounded system case, where equally satisfactory results have been obtained. The effectiveness of the compensation has been

validated by equivalent modeling and extensive simulation runs on the EMTP. These results substantiate what we originally claimed; balanced three phase operation in a two conductor transmission line.

An additional by-product of this research has been the extension and development of a generalized method of analysis for multiple simultaneous faults of the shunt and series variety, built upon transformations of the original bus impedance matrix. Although similar in structure to the method presented by Z.X.Han [6], the proposed algorithm takes advantage of the already formed bus impedance matrix, providing an even greater ease for digital implementation.

Furthermore, the potential of the compensator as a fault limiting device is being explored.

System Model

The system configuration used throughout this dissertation is based on the model presented by Sachdev and Agarwal [7], in order to provide typical system parameter values at the voltage level at which the compensation is realized and the simulations performed. It consists of two large equivalent power systems, represented by two equivalent sources behind their respective impedances interconnected by a transmission line. The transmission line is represented by

a pi section including series impedances and shunt capacitances for the steady state model and by a distributed parameter frequency independent lump resistive model for the dynamic simulation. The line is assumed to be sufficiently transposed so that it may be accurately characterized by its symmetrical sequence impedances. The source impedance as seen from the line terminals is represented by its Thevenin equivalent for a line interconnecting two separate systems, or by an equivalent two port bus impedance network when interconnections, other than the line in question, exist between the remote buses. Shunt capacitors are connected at the bus terminals to represent the capacitance of other transmission lines originating from the same bus and that of the busbar itself. The selective sequence compensator is modeled by a fixed, predetermined, arrangement of passive reactive elements. It is connected into the network, at the sending and receiving busbars, at a specified time during the single pole opening operation.

Transient simulation studies via EMTP (electromagnetic transients program) consider both infinite or ideal sources interconnected by a transmission line and a unit connected synchronous generator against an ideal source. The type-59 [8] dynamic synchronous machine source model was used for simulating the generator. The machine parameters have been obtained from the EMTP benchmark test case # DC-46.

Multi-fault Analysis

Symmetrical Components

A brief review of symmetrical components is included at this point since most of the presented work is built upon this theory. Symmetrical components is the name given to the method or procedure by which an unbalanced system of n-phasors can be resolved into n-systems of balanced phasors called the symmetrical components of the original phasors. In a three phase system the three components are known as the positive, the negative and the zero sequence components.

The positive sequence components are composed of a balanced set of three phasors equal in magnitude and 120° apart and having the same sequence as the original phasors (where it has been assumed that their sequence of rotation is abca...). The negative sequence components are composed of a balanced set of three phase phasors equal in magnitude, 120° apart and of opposite sequence to the original phasors. The zero sequence component is a balanced set of three phase phasors equal in magnitude and co-linear. By transforming each network element of the original system to its sequence component representation it is possible to obtain a network

configuration for each of its symmetrical components. This representation is known as the sequence network and there is one network associated with each sequence component, a positive sequence network, a negative sequence network and a zero sequence network.

By designating as a,b,c the three phases of the system, such that they follow the rotation abca..., that is phase "a" leads phase "b" which leads phase "c", it is possible to decompose them into their symmetrical components.

The positive sequence components of $V_a, V_b, V_c = V^+_a, V^+_b, V^+_c$

The negative sequence components of $V_a, V_b, V_c = V^-_a, V^-_b, V^-_c$

The zero sequence components of $V_a, V_b, V_c = V^0_a, V^0_b, V^0_c$

As stated previously, each original phasor may be expressed as the sum of its components

$$\begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} = \begin{pmatrix} V^+_a \\ V^+_b \\ V^+_c \end{pmatrix} + \begin{pmatrix} V^-_a \\ V^-_b \\ V^-_c \end{pmatrix} + \begin{pmatrix} V^0_a \\ V^0_b \\ V^0_c \end{pmatrix} \qquad (1\text{-}1)$$

and by taking V^+_a, V^-_a, V^0_a, as the reference phasors for each one of the symmetrical sequences, we can write

$$\begin{pmatrix} V^+_b \\ V^-_b \\ V^0_b \end{pmatrix} = \begin{pmatrix} \alpha^2 V^+_a \\ \alpha V^-_a \\ V^0_a \end{pmatrix} = \begin{pmatrix} \alpha^2 V^+ \\ \alpha V^- \\ V^0 \end{pmatrix} \qquad \begin{pmatrix} V^+_c \\ V^-_c \\ V^0_c \end{pmatrix} = \begin{pmatrix} \alpha V^+_a \\ \alpha^2 V^-_a \\ V^0_a \end{pmatrix} = \begin{pmatrix} \alpha V^+ \\ \alpha^2 V^- \\ V^0 \end{pmatrix}$$

(1-2)

where α represents the complex operator e^{j120°.

Substituting in (1-1)

$$\begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} = \begin{pmatrix} V^+ \\ \alpha^2 V^+ \\ \alpha V^+ \end{pmatrix} + \begin{pmatrix} V^- \\ \alpha V^- \\ \alpha^2 V^- \end{pmatrix} + \begin{pmatrix} V^0 \\ V^0 \\ V^0 \end{pmatrix} \tag{1-3}$$

or in matrix form

$$\begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} = \begin{pmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{pmatrix} . \begin{pmatrix} V^0 \\ V^+ \\ V^- \end{pmatrix} = [A] . \begin{pmatrix} V^0 \\ V^+ \\ V^- \end{pmatrix} \tag{1-4}$$

where the inverse relation is

$$\begin{pmatrix} V^0 \\ V^+ \\ V^- \end{pmatrix} = [A]^{-1} . \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \tag{1-5}$$

and

$$[A]^{-1} = \frac{1}{3} . \begin{pmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{pmatrix} \tag{1-6}$$

Similar relations exist for the currents,

$$\begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix} = [A] . \begin{pmatrix} I^0 \\ I^+ \\ I^- \end{pmatrix} \qquad \begin{pmatrix} I^0 \\ I^+ \\ I^- \end{pmatrix} = [A]^{-1} . \begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix}$$

(1-7)

The symmetrical sequence impedance matrix can be obtained from the voltage-current relations in the phase coordinate

$$\begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} = [Z]_{abc} . \begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix}$$

(1-8)

and after substituting the appropriate relations from (1-4) and (1-7)

$$[A] . \begin{pmatrix} V^0 \\ V^+ \\ V^- \end{pmatrix} = [Z]_{abc} . [A] . \begin{pmatrix} I^0 \\ I^+ \\ I^- \end{pmatrix}$$

(1-9)

the desired result is obtained

$$[Z]_{0+-} = [A]^{-1} . [Z]_{abc} . [A]$$

(1-10)

For the cases under consideration, equal self and equal mutual impedances in all three phases, the symmetrical sequence impedance matrix reduces to a diagonal matrix, completely decoupling the sequence networks.

Equations 1-5 and 1-7 resolve three unsymmetrical voltage and current vectors into their symmetrical components. Note that for normal balanced operating conditions, that is abca... sequence, equal phase magnitude and 120° apart, only the positive sequence component is nonzero. To analyze balanced steady state system operation, it is only necessary to deal with the positive sequence network.

Multiple-port Network Theory

A systematic approach to solving multiple faulted networks, based upon multiple-port network theory was presented by Z.X.Han [6]. Every fault point in the system is defined as a port, a pair of terminals such that the current leaving one terminal must equal that entering the other. This condition is satisfied by connecting an ideal transformer between the port and the external connection.

For unbalanced short circuit type faults (phase-ground, phase-phase, phase-phase-ground) the port is located between the faulted phase and the reference in each of the corresponding sequence networks. For unbalanced series type

faults, (one or two phases open), the port is located at each terminal of the unbalance.

The general double fault network is seen in Fig. 1-1. The relationship between the ports is given by:

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \cdot \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} + \begin{pmatrix} V_1^0 \\ V_2^0 \end{pmatrix} \qquad (1\text{-}11)$$

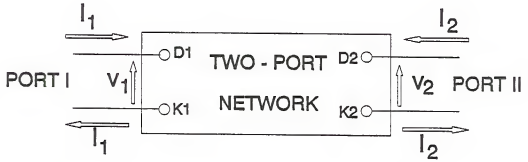

Figure 1-1. Generalized two-port network.

where V_1 and V_2 are the voltages across the two ports with the indicated polarity and I_1 and I_2 represent the respective port currents into and out of each port. The last term in the right corresponds to the open circuit voltage across each port and is nonzero only for the positive sequence representation.

Depending on the type of fault being analyzed, the driving port impedances, Z_{11} and Z_{22} and the transfer impedances, Z_{12} and Z_{21} are computed differently.

For our case of interest, a single pole opening at each end of a line, Z_{11} and Z_{22} are equal to the voltage difference between the two nodes when unit current is applied to one node and flows out of the other. By applying a one per unit current at port one only, it is possible to determine the self driving port impedance. The voltage at port one as given by (1-11) is found to be

$$V_1 = Z_{11} \cdot I_1 = V_{D1} - V_{K1} \tag{1-12}$$

$$V_{D1} = Z_{D1,D1} \cdot I_1 + Z_{D1,K1} \cdot (-I_1) \tag{1-13}$$

where V_{D1} has been obtained by adding the voltages produced at node D1 by the non-zero currents flowing into the network. The negative sign in the second term is used to correct for the defined current direction at node K1. The driving point impedance at node D1 is represented by Z_{D1D1} and Z_{D1K1} constitutes the transfer node impedance between nodes D1 and K1.

Similarly,

$$V_{K1} = Z_{K1K1} \cdot (-I_1) + Z_{D1K1} \cdot (-I_1) \tag{1-14}$$

which when substituted, together with (1-13), into (1-12) results in,

$$V_1 = V_{D1} - V_{K1} = Z_{D1D1} \cdot I_1 + Z_{K1K1} \cdot I_1 - 2 \cdot Z_{D1K1} \cdot I_1 \tag{1-15}$$

from where Z_{11} is obtained

$$Z_{11} = \left(\frac{V_1}{I_1}\right)_{I_2=0} = \frac{V_{D1}-V_{K1}}{I_1=1} = Z_{D1D1} + Z_{K1K1} - 2 \cdot Z_{D1K1}$$

(1-16)

With only a one per unit current injection at the remote port, it is possible to determine the transfer port impedance. The contribution to the port voltage (V_1) due to the current injection at the other port terminals (I_2) is seen to be

$$\begin{aligned} V_1 &= V_{D1} - V_{K1} = Z_{12} \cdot I_2 \\ V_{D1} &= Z_{D2D1} \cdot I_2 + Z_{K2D1} \cdot (-I_2) \\ V_{K1} &= Z_{D2K1} \cdot I_2 + Z_{K2K1} \cdot (-I_2) \end{aligned}$$

(1-17)

where current I_2 flowing into terminal D_2, produces a voltage term at each voltage node equation (V_{D1} and V_{K1}) as well as current $-I_2$ flowing out of terminal K_2.

Substituting in V_1

$$V_1 = (Z_{D2D1} + Z_{K2K1} - Z_{K2D1} - Z_{D2K1}) \cdot I_2$$

(1-18)

from which the transfer impedance between ports one and two is obtained

$$Z_{12} = \frac{V_1}{I_2} = Z_{D2D1} + Z_{K2K1} - Z_{K2D1} - Z_{D2K1}$$

(1-19)

Where Z_{ij} (i,j=D1,D2,K1,K2) corresponds to the transfer impedance between nodes i and j for $i \neq j$ and to the driving

point impedance at node i for i=j. Similarly, the self and transfer port impedances at the second port may be obtained.

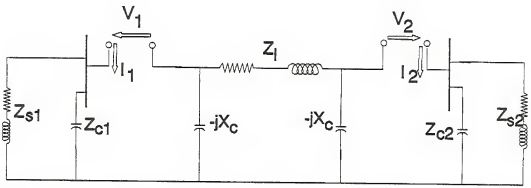

Figure 1-2. Equivalent two-port sequence network of model under single pole opening condition.

The general two-port impedance matrix components, corresponding to our simplified system model can now be derived. The equivalent two-port sequence networks are of the form shown in Fig. 1-2. The required node transfer and self impedances are

$$Z_{D1D1} = \frac{Z_{c1} \cdot Z_{s1}}{Z_{c1} + Z_{s1}}$$

$$Z_{K1K1} = \frac{Z_1 - jX_c}{Z_1 - j2X_c} \cdot (-jX_c)$$

$$Z_{D2D2} = \frac{Z_{c2} \cdot Z_{s2}}{Z_{c2} + Z_{s2}}$$

$$Z_{K1K2} = -\frac{X_c^2}{Z_1 - j2X_c}$$

$$Z_{D1K1} = Z_{D2K2} = Z_{D1K2} = Z_{K2D1} = Z_{D1D2} = Z_{D2K1} = 0$$

(1-20)

from which the elements of the two-port impedance matrix of (1-11) can be formed:

$$Z_{11} = Z_{D1D1} + Z_{K1K1} - 2Z_{D1K1}$$

$$= \frac{Z_{c1} \cdot Z_{s1}}{Z_{c1} + Z_{s1}} - \left(\frac{jX_c \cdot Z_1 + X_c^2}{Z_1 - 2X_c} \right)$$

$$Z_{22} = \frac{Z_{c2} \cdot Z_{s2}}{Z_{c2} + Z_{s1}} - \left(\frac{jX_c \cdot Z_1 + X_c^2}{Z_1 - 2X_c} \right)$$

$$Z_{12} = Z_{21} = -\frac{X_c^2}{Z_1 - 2jX_c}$$

(1-21)

Segregated Sequence Analysis

Even though the faulted (series unbalanced) network may be analyzed by use of multiple port network theory, the transfer impedances required to form the port impedance matrix are not readily available. An extension of the referred method is presented here, by which multiple fault analysis can be easily realized from simple transformations of the bus impedance matrix. The sequence fault current or sequence fault voltage at the port of fault (depending on the type of fault) are represented as current or voltage sources in their respective sequence networks according to the sequence interconnection that is dictated by the type of fault. The corresponding results for parallel and series faults are shown in Tables 1-1 and 1-2.

If the fault boundary conditions require two of the phase currents to be zero (a phase to ground shunt fault, or a two-phase open series fault), the fault is then represented in each sequence network by a current source of appropriate value connected accross each of the corresponding port terminals.

Table 1-1. Parallel fault analysis.

Fault Type	Faulted Phases	Connection Boundary Data	Equivalent Voltage/Current Sources			Solution Boundary Equation
			+ve	-ve	zero	
Phase to Ground	A	$I_b=I_c=0$	I_f	I_f	I_f	$V_a = V^0 + V^+ + V^- = 0$
	C	$I_a=I_b=0$	I_f/α^2	I_f/α	I_f	$V_b = V^0 + \alpha^2V^+ + \alpha V^- =$
	C	$I_a=I_b=0$	I_f/α	I_f/α^2	I_f	$V_c = V^0 + \alpha V^+ + \alpha^2V^- =$
phase to phase	B-C	$V_b=V_c$	V_f	V_f	-	$I_a = I^+ + I^- = 0$
	B-C-g	$V_b=V_c=0$	V_f	V_f	V_f	$I_a = I^0 + I^+ + I^- = 0$
double phase to ground	C-A	$V_c=V_a$	$V_f/(\alpha-1)$	$V_f/(1-\alpha^2)$	-	$I_b = \alpha^2I^+ + \alpha I^- = 0$
	C-A-g	$V_c=V_a=0$	$V_f/(\alpha-1)$	$V_f/(1-\alpha^2)$	$V_f/(\alpha^2-\alpha)$	$I_b = I^0 + \alpha^2I^+ + \alpha I^- = 0$
	A-B	$V_a=V_b$	$V_f/(1-\alpha^2)$	$V_f/(\alpha-1)$	-	$I_c = \alpha I^+ + \alpha^2I^- = 0$
	A-B-g	$V_a=V_b=0$	$V_f/(1-\alpha^2)$	$V_f/(\alpha-1)$	$V_f/(\alpha^2-\alpha)$	$I_c = I^0 + \alpha I^+ + \alpha^2I^- = 0$

If the fault boundary conditions require equality of two of the phase voltages at the fault boundary (a phase to phase and a phase to phase to ground shunt fault, or a single phase open series fault), the fault is represented in each sequence network by a voltage source of appropriate value connected accross each of the corresponding port terminals. The equivalent voltage/current sources are indicated in the following tables for both series and shunt type faults.

Table 1-2. Series fault analysis.

Fault Type	Faulted Phases	Connection Boundary Data	Equivalent Voltage/Current Sources			Solution Boundary Equation
			+ve	-ve	zero	
Single Pole Open	A	$V_b=V_c=0$	V_f	V_f	V_f	$I_a = I^0 + I^+ + I^- = 0$
	B	$V_a=V_b=0$	$V_f/(\alpha-1)$	$V_f/(1-\alpha^2)$	$V_f/(\alpha^2-\alpha)$	$I_b = I^0 + \alpha^2 I^+ + \alpha I^- = 0$
	C	$V_a=V_b=0$	$V_f/(1-\alpha^2)$	$V_f/(\alpha-1)$	$V_f/(\alpha^2-\alpha)$	$I_c = I^0 + \alpha I^+ + \alpha^2 I^- = 0$
Double Pole Open	B-C	$I_b=I_c=0$	I_f	I_f	I_f	$V_a = V^0 + V^+ + V^- = 0$
	C-A	$I_c=I_a=0$	I_f/α^2	I_f/α	I_f	$V_b = V^0 + \alpha^2 V^+ + \alpha V^- = 0$
	A-B	$I_a=I_b$	I_f/α	I_f/α^2	I_f	$V_c=V^0 + \alpha V^+ + \alpha^2 V^-=0$

A procedure to analyze multiple simultaneous faults using the information presented in the previous tables is described next. Multple simultaneous shunt and series faults are first analyzed separately and then combined together.

Multiple shunt faults

Consider first faults involving one or two phases to ground and faults between two or three phases. Depending on whether the fault condition is represented by an equivalent voltage or current source at the fault terminals of each sequence network, the faulted terminals may be classified as type I terminals and type II terminals, respectively. The rows and columns of the bus impedance matrix are next reordered so that the first n faulted buses correspond to type I terminals (phase to ground and three phase faults) and the remaining n+1 through m faulted buses to type II terminals (phase to phase and double phase to ground).

The bus voltages in the positive sequence network, during fault conditions, are composed of that change in voltage due to the flow or injection of fault currents at the faulted nodes and the prefault voltage at the faulted buses, generally assumed to be only of positive sequence content.

$$\begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \\ V_{n+1} \\ \vdots \\ V_m \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} & \cdots & Z_{1n} & Z_{1n+1} & \cdots & Z_{1m} \\ Z_{21} & Z_{22} & \cdots & Z_{2n} & Z_{2n+1} & \cdots & Z_{2m} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ Z_{n1} & Z_{n2} & \cdots & Z_{nn} & Z_{nn+1} & \cdots & Z_{nm} \\ Z_{n+11} & Z_{n+12} & \cdots & Z_{n+1n} & Z_{n+1n+1} & \cdots & Z_{n+1m} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ Z_{m1} & Z_{m2} & \cdots & Z_{mn} & Z_{mn+1} & \cdots & Z_{mm} \end{pmatrix} \cdot \begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_n \\ I_{n+1} \\ \vdots \\ I_m \end{pmatrix} + \begin{pmatrix} V_1^{(0)} \\ V_2^{(0)} \\ \vdots \\ V_n^{(0)} \\ V_{n+1}^{(0)} \\ \vdots \\ V_n^{(0)} \end{pmatrix}$$

(1-22)

Faulted bus voltages are in effect obtained by superposition of the prefault voltages, associated with the flow of load currents, and the change in bus voltage related to the flow of fault currents. In the same sense, total branch currents will be formed by superimposing those obtained from redistribution of the fault current injections at the faulted buses and the prefault load currents. Similar expressions exist for the negative and zero sequence network, with their associated bus impedance values and no prefault voltage term. In general, there is no prefault component of the negative sequence current and voltage in the network, thus the computed values are solely fault induced.

This last equation can be represented in a more compact form

$$\begin{pmatrix} V_I \\ V_{II} \end{pmatrix}_+ = \begin{pmatrix} Z_I & Z_{III} \\ Z_{III} & Z_{II} \end{pmatrix}_+ \cdot \begin{pmatrix} I_I \\ I_{II} \end{pmatrix}_+ + \begin{pmatrix} V_I^{(0)} \\ V_{II}^{(0)} \end{pmatrix}_+$$

(1-23)

Partially inverting the bus impedance matrix to solve for the type II bus fault currents, it is clearly seen that

$$\begin{pmatrix} V_I \\ I_{II} \end{pmatrix}_+ = \begin{pmatrix} \bar{Z}_{II} & K_{III} \\ K_{III} & Y_{III} \end{pmatrix}_+ \cdot \begin{pmatrix} I_I \\ V_{II} \end{pmatrix}_+ + \begin{pmatrix} V_I^{(0)} \\ I_{II}^{(0)} \end{pmatrix}$$

(1-24)

where

$$\tilde{Z}_{II} = Z_{II} - Z_{III} \cdot Z_{III}^{-1} \cdot Z_{III}$$
$$K_{III} = -Z_{III}^{-1} \cdot Z_{III}$$
$$Y_{III} = Z_{III}^{-1}$$
$$I_{II}^{(0)} = -Z_{III}^{-1} \cdot V_{II}^{(0)}$$

(1-25)

similar expressions are obtained for the negative and zero sequence networks

$$\begin{pmatrix} V_I \\ I_{II} \end{pmatrix}_- = \begin{pmatrix} \tilde{Z}_{II} & K_{III} \\ K_{III} & Y_{III} \end{pmatrix}_- \cdot \begin{pmatrix} I_I \\ V_{II} \end{pmatrix}_-$$

(1-26)

$$\begin{pmatrix} V_I \\ I_{II} \end{pmatrix}_0 = \begin{pmatrix} \tilde{Z}_{II} & K_{III} \\ K_{III} & Y_{III} \end{pmatrix}_0 \cdot \begin{pmatrix} I_I \\ V_{II} \end{pmatrix}_0$$

(1-27)

Enforcing the additional boundary conditions as determined by fault type, and shown under column "Solution Boundary Equation" in Tables 1-1 and 1-2, we can write

$$\sum_{i=+,-,0} [\Pi]_i \cdot \begin{pmatrix} V_I \\ I_{II} \end{pmatrix}_i = (0)$$

(1-28)

where $[n]_{i=+,-,0}$ for each sequence network is a diagonal matrix whose element n_{jj} corresponds to the complex coefficient (shown in Tables 1-1 and 1-2) of the equivalent voltage/current source (V_f,I_f) associated to the type of shunt fault at bus j. Expanding the summation

$$[n]_+ \cdot \begin{pmatrix} V_I \\ I_{II} \end{pmatrix}_+ + [n]_- \cdot \begin{pmatrix} V_I \\ I_{II} \end{pmatrix}_- + [n]_0 \cdot \begin{pmatrix} V_I \\ I_{II} \end{pmatrix}_0 = [0] \tag{1-29}$$

and substituting (1-23),(1-26) and (1-27) into this last equation we obtain

$$[n]_+ \cdot \begin{pmatrix} \bar{Z}_{II} & K_{III} \\ K_{III} & Y_{III\,III} \end{pmatrix}_+ \cdot \begin{pmatrix} I_I \\ V_{II} \end{pmatrix}_+ + [n]_- \cdot \begin{pmatrix} \bar{Z}_{II} & K_{III} \\ K_{III} & Y_{III\,III} \end{pmatrix}_- \cdot \begin{pmatrix} I_I \\ V_{II} \end{pmatrix}_- +$$

$$[n]_0 \cdot \begin{pmatrix} \bar{Z}_{II} & K_{III} \\ K_{III} & Y_{III\,III} \end{pmatrix}_0 \cdot \begin{pmatrix} I \\ V_{II} \end{pmatrix}_0 + [n]_+ \cdot \begin{pmatrix} V_I^{(0)} \\ I_{II}^{(0)} \end{pmatrix}_+ = [0] \tag{1-30}$$

The voltages and currents in the above expression are related to one another according to the connection boundary data as listed in the previous tables. It is seen that

$$\begin{pmatrix} I_I \\ V_{II} \end{pmatrix}_+ = [m]_+ \cdot \begin{pmatrix} I_f \\ V_f \end{pmatrix}$$

$$\begin{pmatrix} I_I \\ V_{II} \end{pmatrix}_- = [m]_- \cdot \begin{pmatrix} I_f \\ V_f \end{pmatrix}$$

$$\begin{pmatrix} I_I \\ V_{II} \end{pmatrix}_0 = [m]_0 \cdot \begin{pmatrix} I_f \\ V_f \end{pmatrix} \tag{1-31}$$

where $[m]_+$, $[m]_-$ and $[m]_0$ are all diagonal matrices with complex elements as required by the "Equivalent Voltage/Current Sources" column of the referred tables.

Substituting and solving for the common terms, we obtain

$$\begin{pmatrix} I_f \\ V_f \end{pmatrix} = -\left([n]_+ \cdot \begin{pmatrix} \bar{Z}_{II} & K_{III} \\ K_{III} & Y_{IIII} \end{pmatrix}_+ \cdot [m]_+ + [n]_- \cdot \begin{pmatrix} \bar{Z}_{II} & K_{III} \\ K_{III} & Y_{IIII} \end{pmatrix}_- \cdot [m]_- + [n]_0 \cdot \begin{pmatrix} \bar{Z}_{II} & K_{III} \\ K_{III} & Y_{IIII} \end{pmatrix}_0 \cdot [m]_0 \right)^{-1} \cdot [n]_+ \cdot \begin{pmatrix} V_I^{(0)} \\ I_{II}^{(0)} \end{pmatrix}_+ \qquad (1\text{-}32)$$

from which the required sequence components for determining the phase quantities may be evaluated.

Multiple series faults

When only series faults are considered, depending on the required interconnection of the sequence networks, faults may be further subdivided into type I_s (Single Pole Openings, SPO) and type II_s (Double Pole Openings, DPO). Each port associated to a series fault has two corresponding buses (excluding the reference), one on each side of the fault. For a single series fault at port K, with associated buses K_1 and K_2 the

corresponding bus voltage equations for the positive sequence network are

$$V_{k1} = Z_{k1,1} \cdot I_1 + Z_{k1,2} \cdot I_2 + \ldots + Z_{k1,k1} \cdot I_{k1} + Z_{k1,k2} \cdot I_{k2} + \ldots + Z_{k1,m} \cdot I_m + V_{k1}^{(0)}$$

$$V_{k2} + Z_{k2,1} \cdot I_2 + Z_{k2,2} \cdot I_2 + \ldots + Z_{k2,k1} \cdot I_{k1} + Z_{k2,k2} \cdot I_{k2} + \ldots + Z_{k2,m} \cdot I_m + V_{k2}^{(0)}$$

(1-33)

where the currents $I_{j \neq k1,k2}$ represent current injections due to faults at those buses. Similar expressions exist for the negative and zero sequence networks, excluding the prefault voltage terms.

Because of the current requirement that characterizes a port in an electric circuit, it is known that $I_k = I_{k2} = -I_{k1}$. Substituting, the voltage across the port is found to be

$$V_k = V_{k1} - V_{k2} = (Z_{k1,1} - Z_{k2,1}) \cdot I_1 + (Z_{k1,2} - Z_{k2,2}) \cdot I_2 + \ldots + (Z_{k1,k1} - Z_{k2,k1} + Z_{k2,k2} - Z_{k1,k2}) \cdot I_k + \ldots + (Z_{k1,m} - Z_{k2,m}) \cdot I_m + \left(V_{k1}^{(0)} - V_{k2}^{(0)}\right)$$

(1-34)

where the $Z_{i,j}$ are the self and transfer bus impedances for the positive sequence network, with the series faults (line openings) represented as a discontinuity in the sequence network, with two associated bus terminals per series fault.

To obtain the $Z_{i,j}$ terms to be used in the above equations, it is necessary to modify the original Z_{bus}

impedance matrix, that is the impedance associated with the system under no fault conditions. Standard algorithms used in forming the Z_{bus} impedance matrix may be applied for this purpose. When adding a new branch (Z_b) between two existing buses, k and m, the new bus impedance matrix can be obtained from

$$Z_{bus(new)} = Z_{bus(old)} - \frac{1}{Z_b + Z_{kk} + Z_{mm} - 2Z_{km}} \cdot \begin{pmatrix} Z_{1k} - Z_{1m} \\ Z_{2k} - Z_{2m} \\ \vdots \\ Z_{nk} - Z_{nm} \end{pmatrix} \cdot \left((Z_{1k} - Z_{1m}) \ \cdots \ (Z_{nk} - Z_{nm}) \right) \tag{1-35}$$

Also, adding a new branch (Z_b) from an old bus k to a new bus p is equivalent to

$$Z_{bus(new)} = \begin{pmatrix} & & & Z_{1k} \\ & Z_{bus(old)} & & Z_{2k} \\ & & & \vdots \\ & & & Z_{nk} \\ Z_{1k} & Z_{2k} & \cdots Z_{nk} & Z_{kk} + Z_b \end{pmatrix} \tag{1-36}$$

Series faults at one end of a line only may then be represented in the bus impedance matrix as an inverse procedure to that used in adding a line between two existing buses and that used to represent the addition of a new busthrough an impedance to an existing bus. With reference to (1-34), Zbus(new) can be taken to represent the original impedance matrix. Solving for $Z_{bus(old)}$ then represents the effect of removing the faulted line. Modifying $Z_{bus(old)}$ per

(1-35) will then render the bus impedance matrix under a series fault at one end of a line. Finding the equivalent Z_{bus} matrix under multiple series fault conditions, may be accomplished by sequential application of the described procedure to the original matrix. It was assumed in the above equations that the line impedance was adequately represented by a single series element. When determining the modified bus impedance matrix subject to series faults, more complex representations of the line involving shunt capacitances to ground may also be considered by use of other variants in the Z_{bus} forming algorithm.

In general, for m series type simultaneous faults, the corresponding bus voltages of the positive sequence network, in terms of the bus impedance matrix, may be represented as

$$\begin{pmatrix} V_{1a} \\ V_{1b} \\ V_{2a} \\ V_{2b} \\ \vdots \\ \vdots \\ V_{ma} \\ V_{mb} \end{pmatrix} = \begin{pmatrix} Z_{1a,1a} & Z_{1a,1b} & Z_{1a,2a} & Z_{1a,2b} & \cdots & \cdots & Z_{1a,ma} & Z_{1a,mb} \\ Z_{1b,1a} & Z_{1b,1b} & Z_{1b,2a} & Z_{1b,2b} & \cdots & \cdots & Z_{1b,ma} & Z_{1b,mb} \\ Z_{2a,1a} & Z_{2a,1b} & \cdots & \cdots & \cdots & \cdots & Z_{2a,ma} & Z_{2a,mb} \\ Z_{2b,1a} & Z_{2b,1b} & \cdots & \cdots & \cdots & \cdots & Z_{2b,ma} & Z_{2b,mb} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ Z_{ma,1a} & Z_{ma,1b} & Z_{ma,2a} & Z_{ma,2b} & \cdots & \cdots & Z_{ma,ma} & Z_{ma,mb} \\ Z_{mb,1a} & Z_{mb,1b} & Z_{mb,2a} & Z_{mb,2b} & \cdots & \cdots & Z_{mb,ma} & Z_{mb,mb} \end{pmatrix} \cdot \begin{pmatrix} I_{1a} \\ I_{1b} \\ I_{2a} \\ I_{2b} \\ \vdots \\ \vdots \\ I_{ma} \\ I_{mb} \end{pmatrix} + \begin{pmatrix} V_{1a}^{(0)} \\ V_{1b}^{(0)} \\ V_{2a}^{(0)} \\ V_{2b}^{(0)} \\ \vdots \\ \vdots \\ V_{ma}^{(0)} \\ V_{mb}^{(0)} \end{pmatrix} \tag{1-37}$$

where the associated bus terminals for each one of the m ports have been designated "a" and "b". To reduce this expression

to that corresponding to port voltages and currents, the bus equation associated to terminal b of each port is substracted from that of terminal a, obtaining

$$\begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ \vdots \\ V_m \end{pmatrix} = \begin{pmatrix} V_{1a} - V_{1b} \\ V_{2a} - V_{2b} \\ \vdots \\ \vdots \\ V_{ma} - V_{mb} \end{pmatrix} = \begin{pmatrix} (Z_{1a,1a}-Z_{1b,1a}) & (Z_{1a,1b}-Z_{1b,1b}) & \cdots & \cdots & (Z_{1a,mb}-Z_{1b,mb}) \\ (Z_{2a,1a}-Z_{2b,1a}) & (Z_{2a,1b}-Z_{2b,1b}) & \cdots & \cdots & (Z_{2a,mb}-Z_{2b,mb}) \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ (Z_{ma,1a}-Z_{mb,1a}) & (Z_{ma,1b}-Z_{mb,1b}) & \cdots & \cdots & (Z_{ma,mb}-Z_{mb,mb}) \end{pmatrix} \cdot \begin{pmatrix} I_{1a} \\ I_{1b} \\ \vdots \\ \vdots \\ I_{mb} \end{pmatrix}$$

$$+ \begin{pmatrix} V_{1a}^{(0)} - V_{1b}^{(0)} \\ V_{2a}^{(0)} - V_{2b}^{(0)} \\ \vdots \\ \vdots \\ V_{ma}^{(0)} - V_{mb}^{(0)} \end{pmatrix} \qquad (1\text{-}38)$$

which can be reduced for ease of handling to

$$\begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ \vdots \\ V_m \end{pmatrix} = \begin{pmatrix} Z_{1,1a} & Z_{1,1b} & Z_{1,2a} & Z_{1,2b} & \cdots & \cdots & Z_{1,ma} & Z_{1,mb} \\ Z_{2,1a} & Z_{2,1b} & Z_{2,2a} & Z_{2,2b} & \cdots & \cdots & Z_{2,ma} & Z_{2,mb} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ Z_{m,1a} & Z_{m,1b} & Z_{m,2a} & Z_{m,2b} & \cdots & \cdots & Z_{m,ma} & Z_{m,mb} \end{pmatrix} \cdot \begin{pmatrix} I_{1a} \\ I_{1b} \\ I_{2a} \\ I_{2b} \\ \vdots \\ \vdots \\ I_{ma} \\ I_{mb} \end{pmatrix} + \begin{pmatrix} V_1^{(0)} \\ V_2^{(0)} \\ \vdots \\ \vdots \\ V_m^{(0)} \end{pmatrix}$$

(1-39)

and making use of the remaining requirement on the port currents

$$\begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ \vdots \\ I_m \end{pmatrix} = \begin{pmatrix} I_{1a} \\ I_{2a} \\ \vdots \\ \vdots \\ I_{ma} \end{pmatrix} = - \begin{pmatrix} I_{1b} \\ I_{2b} \\ \vdots \\ \vdots \\ I_{mb} \end{pmatrix}$$

(1-40)

in terms of (1-39), this last one is equivalent to substracting each odd numbered column of the modified Z_{bus} matrix from its lower even numbered column. The port voltages are now

$$\begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_m \end{pmatrix} = \begin{pmatrix} (Z_{1,1a}-Z_{1,1b}) & (Z_{1,2a}-Z_{1,2b}) & \cdots & (Z_{1,ma}-Z_{1,mb}) \\ (Z_{2,1a}-Z_{2,1b}) & (Z_{2,2a}-Z_{2,2b}) & \cdots & (Z_{2,ma}-Z_{2,mb}) \\ \cdots & \cdots & \cdots & \cdots \\ (Z_{m,1a}-Z_{m,1b}) & (Z_{m,2a}-Z_{m,2b}) & \cdots & (Z_{m,ma}-Z_{m,mb}) \end{pmatrix} \cdot \begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_m \end{pmatrix} + \begin{pmatrix} V_1^{(0)} \\ V_2^{(0)} \\ \vdots \\ V_m^{(0)} \end{pmatrix}$$

(1-41)

Let ports 1 through n, correspond to type I_s, those where the fault condition may be represented by an equivalent voltage source across the port terminals, and let ports (n+1) through m, belong to type II_s, those for which the fault condition may be represented by an equivalent current source across the port terminals. Proceeding as before, it is possible to obtain a similar expression to that of (1-24)

$$\begin{pmatrix} V_I \\ I_{II} \end{pmatrix} = \begin{pmatrix} \bar{Z}_{II} & K_{III} \\ K_{III} & Y_{III} \end{pmatrix} \cdot \begin{pmatrix} I_I \\ V_{II} \end{pmatrix} + \begin{pmatrix} V_I^{(0)} \\ I_{II}^{(0)} \end{pmatrix}$$

(1-42)

voltages and currents are now series port quantities, and the elements of the impedance matrix have been obtained through a

sequence of transformations on the original Z_{bus} impedance matrix, as previously described. Equations of the same structure can be derived for the negative and zero sequence networks, with the exception of the prefault voltage/current term which generally has a zero value. Satisfying the solution boundary conditions, as listed in Table 1-2 under solution boundary equation according to the specific series fault types and involved phases, expressions analogous to those in (1-28) through (1-31) can be obtained, with a solution of the same structure as that of (1-32) for the currents and voltages of the types I_s and II_s faulted series ports.

Generalized multiple faults

Consider a system with k simultaneous faults, where $k = m_p + n_p + m_s + n_s$, the total of class I and II shunt and series type faults respectively; m_p and m_s are the number of type I class faults in each subdivision (shunt and series),that is, faults that may be represented by an equivalent current source, flowing into and out of the faulted terminals in the corresponding sequence networks (single line to ground and double pole openings, as per Tables 1-1,1-2); n_p and n_s are the number of type II class faults in each subdivision that may be represented by an equivalent voltage source connected accross the faulted terminals in the sequence networks (double phase, double phase to ground and single line

open). The general equation describing the faulted system, can be obtained from

$$\begin{pmatrix} V_{I_p} \\ V_{I_s} \\ V_{II_p} \\ V_{II_s} \end{pmatrix}_i = \begin{pmatrix} Z_{I_pI_p} & Z_{I_pI_s} & Z_{I_pII_p} & Z_{I_pII_s} \\ Z_{I_sI_p} & Z_{I_sI_s} & Z_{I_sII_p} & Z_{I_sII_s} \\ Z_{II_pI_p} & Z_{II_pI_s} & Z_{II_pII_p} & Z_{II_pII_s} \\ Z_{II_sI_p} & Z_{II_sI_s} & Z_{II_sII_p} & Z_{II_sII_s} \end{pmatrix}_i \cdot \begin{pmatrix} I_{I_p} \\ I_{I_s} \\ I_{II_p} \\ I_{II_s} \end{pmatrix}_i + \begin{pmatrix} V_{I_p}^{(0)} \\ V_{I_s}^{(0)} \\ V_{II_p}^{(0)} \\ V_{II_s}^{(0)} \end{pmatrix}_i$$

$$(i=0,+,-)$$

(1-43)

The vectors of bus voltages with class I and class II type parallel faults are represented by V_{Ip} and V_{IIp} respectively. The vectors of bus voltages under class I and class II type series faults are represented by V_{Is} and V_{IIs} respectively. A similar description is valid for the current vectors. This equation characterizes the system under simultaneous multiple series and shunt type fault states in the positive, negative and zero sequence networks, as indicated by the subscript i. The prefault voltage term, in the extreme right hand side of the equation, is generally assumed to be zero for the negative and zero sequence networks. This is equivalent to assuming a balanced three phase system prior to the fault occurrence.

The bus impedance matrix in the above equation has been ordered, so that the first m_p rows correspond to buses with class I shunt or parallel type faults, followed by m_s rows of buses with class I series type faults. Next, the faulted

buses with class II type faults, n_p shunt or parallel types followed by n_s series type. Note that this matrix has been obtained from the original bus impedance matrix associated with the faulted buses after the operations associated to line openings (series faults) have been performed as indicated previously in (1-35). Each bus associated to a series fault is only one of a pair describing the faulted port; the bus at which current injection is defined into the network is listed first.

Forming the port voltages for each series faults (both of Class I and II), is easily achieved by substraction of the associated buses, as shown in (1-37). This can be represented by an elementary row transformation of the impedance matrix

$$\begin{pmatrix} V_{I_p} \\ \dot{V}_{I_s} \\ V_{II_p} \\ \dot{V}_{II_s} \end{pmatrix}_i = [R_1] \cdot \begin{pmatrix} Z_{I_pI_p} & Z_{I_pI_s} & Z_{I_pII_p} & Z_{I_pII_s} \\ Z_{I_sI_p} & Z_{I_sI_s} & Z_{I_sII_p} & Z_{I_sII_s} \\ Z_{II_pI_p} & Z_{II_pI_s} & Z_{II_pII_p} & Z_{II_pII_s} \\ Z_{II_sI_p} & Z_{II_sI_s} & Z_{II_sII_p} & Z_{II_sII_s} \end{pmatrix}_i \cdot \begin{pmatrix} I_{I_p} \\ I_{p_s} \\ I_{II_p} \\ I_{II_s} \end{pmatrix}_i + \begin{pmatrix} V_{I_p}^{(0)} \\ \dot{V}_{I_s}^{(0)} \\ V_{II_p}^{(0)} \\ \dot{V}_{II_s}^{(0)} \end{pmatrix}_i$$

$$(i=0,+,-) \qquad (1\text{-}44)$$

where the dimension of vectors V'_{Is} and V'_{IIs} have been reduced by one half, on account of the elementary operation indicated in (1-37). The voltages at the series fault locations, for both class I and class II type faults, now represent the voltage across the series port, or open terminal(s) in the sequence networks. The final transformation required to obtain

the corresponding series port voltages in terms of their corresponding port currents can be effected through an elementary column transformation, similar to that implied in (1-40)

$$\begin{pmatrix} V_{I_p} \\ \acute{V}_{I_s} \\ V_{II_p} \\ \acute{V}_{II_s} \end{pmatrix}_i = [R_1] \cdot \begin{pmatrix} Z_{I_pI_p} & Z_{I_pI_s} & Z_{I_pII_p} & Z_{I_pII_s} \\ Z_{I_sI_p} & Z_{I_sI_s} & Z_{I_sII_p} & Z_{I_sII_s} \\ Z_{II_pI_p} & Z_{II_pI_s} & Z_{II_pII_p} & Z_{II_pII_s} \\ Z_{II_sI_p} & Z_{II_sI_s} & Z_{II_sII_p} & Z_{II_sII_s} \end{pmatrix}_i \cdot [C_1] \cdot \begin{pmatrix} I_{I_p} \\ \acute{I}_{I_s} \\ I_{II_p} \\ \acute{I}_{II_s} \end{pmatrix}_i + \begin{pmatrix} V^{(0)}_{I_p} \\ \acute{V}^{(0)}_{I_s} \\ V^{(0)}_{II_p} \\ \acute{V}^{(0)}_{II_s} \end{pmatrix}_i$$

$$(i=0,+,-) \qquad (1\text{-}45)$$

The port currents at the series fault locations, I'_{Is} and I'_{IIs}, also have their dimension reduced by half. The system equations may now be represented by

$$\begin{pmatrix} V_{I_p} \\ \acute{V}_{I_s} \\ V_{II_p} \\ \acute{V}_{II_s} \end{pmatrix}_i = \begin{pmatrix} Z_{I_pI_p} & \acute{Z}_{I_pI_s} & Z_{I_pII_p} & \acute{Z}_{I_pII_s} \\ \acute{Z}_{I_sI_p} & \acute{Z}_{I_sI_s} & \acute{Z}_{I_sII_p} & \acute{Z}_{I_sII_s} \\ Z_{II_pI_p} & \acute{Z}_{II_pI_s} & Z_{II_pII_p} & \acute{Z}_{II_pII_s} \\ \acute{Z}_{II_sI_p} & \acute{Z}_{II_sI_s} & \acute{Z}_{II_sII_p} & \acute{Z}_{II_sII_s} \end{pmatrix}_i \cdot \begin{pmatrix} I_{I_p} \\ \acute{I}_{I_s} \\ I_{II_p} \\ \acute{I}_{II_s} \end{pmatrix}_i + \begin{pmatrix} V^{(0)}_{I_p} \\ \acute{V}^{(0)}_{I_s} \\ V^{(0)}_{II_p} \\ \acute{V}^{(0)}_{II_s} \end{pmatrix}_i$$

$$(i=0,+,-) \qquad (1\text{-}46)$$

and the primes indicate the original vectors and submatrices of (1-42) being modified by the prescribed transformations.

Partially inverting the modified bus impedance matrix to solve for the type II shunt bus and series fault currents, one obtains

$$\begin{pmatrix} V_{I_p} \\ \acute{V}_{I_s} \\ I_{II_p} \\ \acute{I}_{II_s} \end{pmatrix}_i = \begin{pmatrix} \bar{Z}_{I_pI_p} & \bar{Z}_{I_pI_s} & K_{I_pII_p} & K_{I_pII_s} \\ \bar{Z}_{I_sI_p} & \bar{Z}_{I_sI_s} & K_{I_sII_p} & K_{I_sII_s} \\ K_{II_pI_p} & K_{II_pI_s} & Y_{II_pII_p} & Y_{II_pII_s} \\ K_{II_sI_p} & K_{II_sI_s} & Y_{II_sII_p} & Y_{II_sII_s} \end{pmatrix}_i \cdot \begin{pmatrix} I_{I_p} \\ \acute{I}_{I_s} \\ V_{II_p} \\ \acute{V}_{II_s} \end{pmatrix}_i + \begin{pmatrix} V_{I_p}^{(0)} \\ \acute{V}_{I_s}^{(0)} \\ I_{II_p}^{(0)} \\ \acute{I}_{II_s}^{(0)} \end{pmatrix}_i$$

$$(i=0,+,-) \qquad (1\text{-}47)$$

where the prefault voltage and current term is non-zero only for the positive sequence network equation. Satisfying the additional boundary conditions according to the type of fault, as indicated in Tables 1-1 and 1-2, and proceeding as before, an equation of the form of (1-32) is obtained for the common terms I_f and V_f. These now represent the intermediate or common values of sequence currents entering the series and parallel ports for the class I faults, and of sequence voltages across the series and parallel ports for the class II faults. Back substitution completely solves the system.

CHAPTER 2
SELECTIVE SEQUENCE FILTERING

In this chapter, a new shunt compensator arrangement is presented which can be used to selectively filter the negative and zero sequence components of the line current in a typical extra high voltage (EHV) system during unbalanced conditions.

Generally, shunt compensators have been employed for load compensation, to balance real power and reduce or cancel reactive power drawn by large loads, usually in industrial installations and distribution circuits. Shunt compensators are also used to provide voltage support to transmission lines, where the objective is to regulate or control the voltage at a given terminal, improving system response to disturbances and assisting in the steady state operation of the system. Transient and dynamic stability of the system can also benefit from adequate reactive compensation.

L.Gyugyi et al. [9] examine the theoretical foundations of thyristor-controlled shunt compensation, conditions for unbalanced load compensation (for a delta or ungrounded three phase load) and voltage stabilization are established with the use of symmetrical components.

This dissertation introduces a new shunt compensator model, of the variable impedance type (one that functions as a variable capacitive and inductive reactance), which can be used during the single pole opening (SPO) condition to prevent the flow of the negative and the zero sequence components of the line current into the associated remote systems of a transmission line. The proposed compensator is in essence a load compensator that converts the unbalanced three phase load seen from the line terminals, by the remote systems, into a balanced three phase load. By presenting a low impedance path to the flow of these sequence components, the negative and zero sequence currents are prevented from flowing into the remote systems. The unbalanced currents generated by the open pole condition, are effectively nullified in the sense that they are not seen by the remote systems behind the terminal buses of the affected line, but are now limited to circulate through the sequence filters and the affected line.

The concept of sequence current recirculation is, to the author's knowledge, an original contribution to the field of power systems operation and control. Its application to SPO conditions is a first logical benefit of this idea.

Basic Concepts of Load Compensation.

An ungrounded wye connected unbalanced load can be represented by its delta connected equivalent. Consider, for convenience, the admittance representation of the load Y_{ab}, Y_{bc} and Y_{ca} and assume that the load is supplied by a set of positive sequence phase to neutral voltages $V_a = V$, $Vb = Ve^{-j2\pi/3}$ and $V_c = Ve^{j2\pi/3}$ as depicted in Fig.2-1.

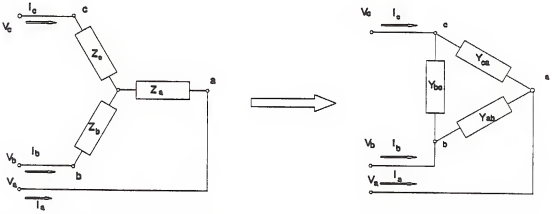

Figure 2-1 General ungrounded wye impedance load and its delta admittance equivalent.

The three delta equivalent admittances can be compensated separately as if they were three single phase loads. Let us first consider the load connected across phases ab. Expressing Y_{ab} by its real (conductance) and imaginary (susceptance) components

$$Y_{ab} = G_{ab} + jB_{ab} \qquad (2\text{-}1)$$

It is readily seen that the reactive portion of this branch can be compensated by paralleling it with a susceptance of the same magnitude and opposite sign.

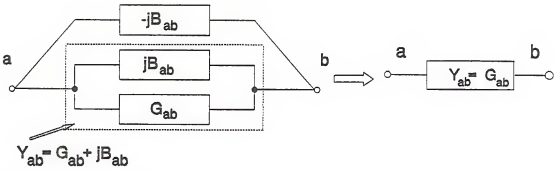

Figure 2-2. Reactive compensation of admittance branch Y_{ab}.

As a second step of the compensation the conductance G_{ab} has to be complemented with a reactive network in order to obtain a balanced load on the ac supply. The basic criteria for this compensation are that,

1) No additional reactive power flow needs are created by the compensation, as seen from the line terminals of the load. The load has, in effect, become of purely resistive composition.
2) A balanced three phase real power of the same magnitude as that of the equivalent single phase load (G_{ab}) is obtained. Real power requirements are unchanged after compensation.

The general compensating network, for the single phase load G_{ab} (the conductance between phases a and b of delta or ungrounded load) is shown in Fig.2-3 below

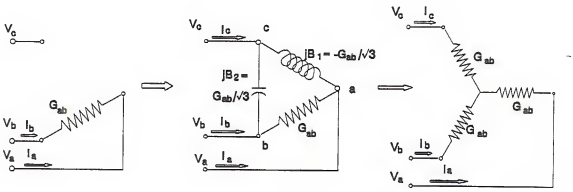

Figure 2-3. Reactive compensation and equivalence of the branch A-B conductance.

The real power supplied by the ac source to the equivalent single phase load connected across phases a and b, prior to the compensation, is

$$P = (\sqrt{3}\,V)^2 G_{ab} = 3\,V^2 G_{ab} \qquad (2\text{-}2)$$

The balanced real power requirement demands that a third of the real power supplied to the equivalent single phase load be supplied by each phase. The real power per phase, under compensation is now V^2G_{ab}. The reactive power constraints translate to each line current being in phase with its corresponding voltage.

The new line current in phase A, from the partially compensated network (Fig.2-3), can be readily obtained

$$I_{a_c} = V_{ab}G_{ab} - V_{ca}jB_1$$
$$= \sqrt{3}\,VG_{ab}e^{j30^\circ} - \sqrt{3}\,VB_1 e^{j(150^\circ+90^\circ)}$$

(2-3)

The reactive constraint for phase A, requires that the compensated line A current I_{ac} have a zero imaginary part (taking the phase A voltage to be at zero degrees).

$$Imaginary[I_{a_c}] = 0$$
$$\sqrt{3}\,VG_{ab}\sin 30^\circ - \sqrt{3}\,VB_1 \sin 240^\circ = 0$$
$$\sqrt{3}\,VG_{ab}\left(\frac{1}{2}\right) - \sqrt{3}\,VB_1\left(-\frac{\sqrt{3}}{2}\right) = 0$$

(2-4)

from which the required compensating susceptance B_1 is derived

$$B_1 = -\frac{G_{ab}}{\sqrt{3}}$$

(2-5)

where the negative sign corresponds to an inductor of the indicated magnitude. It is seen that the requirement on the real power for the phase A is automatically satisfied

$$Real[I_{a_c}] = \sqrt{3}\,VG_{ab}Cos30^\circ - \sqrt{3}\,VB_1 Cos240^\circ$$
$$= \frac{3}{2}VG_{ab} - \frac{1}{2}VG_{ab}$$
$$= VG_{ab}$$

(2-6)

which provides one third of the originally supplied real power to the equivalent single phase load

$$(RealPower)_{phase\,A} = V_a I_{a_c} Cos\theta_a = V^2 G_{ab}$$

(2-7)

where θ_a denotes the angle between phase A voltage and current.

Similarly, the line current in phase B is now

$$\begin{aligned} I_{b_c} &= -V_{ab}G_{ab} - V_{bc}jB_2 \\ &= -\sqrt{3}\,VG_{ab}e^{j30^\circ} + \sqrt{3}\,VB_2\,e^{j(90^\circ+(-90^\circ))} \end{aligned}$$

(2-8)

multiplying I_b through by e^{j120° allows dealing with the real and imaginary parts of the resulting expression as the in phase and quadrature components (with respect to V_b) of the phase B current. The requirement of zero reactive power supplied by the line is satisfied if

$$\begin{aligned} &Imaginary\,[I_{b_c}e^{j120^\circ}] = 0 \\ &-\sqrt{3}\,VG_{ab}Sin(150^\circ) + \sqrt{3}\,VB_2Sin(120^\circ) = 0 \\ &-\frac{\sqrt{3}}{2}\,VG_{ab} + \sqrt{3}\,VB_2\,(\frac{\sqrt{3}}{2}) = 0 \end{aligned}$$

(2-9)

from which the compensating element B_2 can be obtained

$$B_2 = \frac{G_{ab}}{\sqrt{3}}$$

(2-10)

where the positive value indicates a capacitive element of the specified magnitude.

The real power requirement for phase B is seen to be simultaneously satisfied

$$\begin{aligned} Real\,[I_{b_c} e^{j120°}] &= -\sqrt{3}\,VG_{ab}\,Cos(150°) + \sqrt{3}\,VB_2\,Cos(120°) \\ &= \frac{3}{2}\,VG_{ab} - (\frac{\sqrt{3}}{2})\,V\frac{G_{ab}}{\sqrt{3}} \\ &= VG_{ab} \end{aligned} \qquad (2\text{-}11)$$

providing one third of the originally supplied real power to the equivalent single phase load of phase A

$$(RealPower)_{phaseB} = V_b I_{b_c} Cos\theta_b = V^2 G_{ab} \qquad (2\text{-}12)$$

with θ_b representing the angle between phase B voltage and current. Once phases A and B have been balanced through reactive compensation (for this single phase load), as has been previously proven, the requirements on the phase C current are automatically satisfied. This is due to the nature of the load being compensated, delta or ungrounded wye, which prevents the flow of zero sequence components of the current from the line. Consequently, the phase C current balances out the summation of the phase A and phase B currents and provides the remaining third of the real power required by the equivalent load.

Proceeding as before, the susceptance terms of the corresponding delta loads in the other two branches (Fig.2-1), jB_{bc} and jB_{ca}, can be readily compensated through susceptances of corresponding magnitude and opposite sign. It is also

possible to derive compensators for the unbalanced conductances of the associated delta branches, G_{bc} and G_{ca}. This compensation can be effected by paralleling inductive susceptances of magnitude $G_{bc}/\sqrt{3}$ and $G_{ca}/\sqrt{3}$ across the terminals associated to the leading delta voltages to the B-C and C-A branches, V_{ab} and V_{bc} respectively, and by paralleling capacitive susceptances of magnitude $G_{bc}/\sqrt{3}$ and $G_{ca}/\sqrt{3}$ across the terminals associated to the lagging delta voltage to the referred branches, V_{ca} and V_{bc} respectively.

Figures 2-4 and 2-5, respectively, depict the required compensation for the B-C leg of the equivalent delta load, and that corresponding to the A-C branch with their equivalent real balanced representation

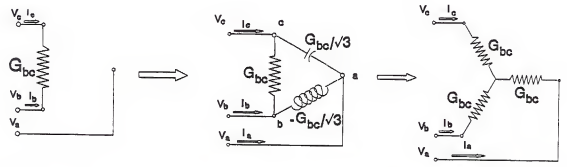

Figure 2-4. Reactive compensation and equivalence of the branch B-C conductance.

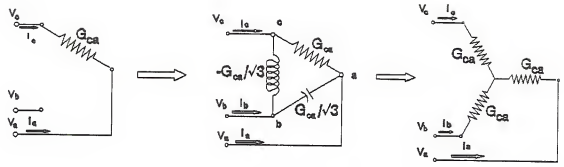

Figure 2-5. Reactive compensation and equivalence of the branch C-A conductance.

The compensation required to convert an unbalanced three phase delta or ungrounded load to a balanced one, at unity power factor, can then be achieved by adding all compensating susceptances in each phase or delta branch. The equivalent circuit then becomes

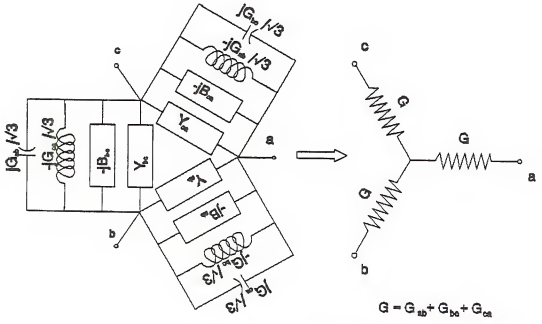

Figure 2-6.Complete reactive compensation to an unbalanced ungrounded load.

The compensating reactances to be connected across the branches of the equivalent delta loads are

$$B_{ab}^{comp} = -B_{ab} + \frac{(G_{ca} - G_{bc})}{\sqrt{3}}$$

$$B_{bc}^{comp} = -B_{bc} + \frac{(G_{ab} - G_{ca})}{\sqrt{3}}$$

$$B_{ca}^{comp} = -B_{ca} + \frac{(G_{bc} - G_{ab})}{\sqrt{3}}$$

(2-13)

This compensator has in fact filtered out of the line the negative sequence components of the load current drawn by the unbalanced load and provided enough reactive power support to present an equivalent balanced real load to the system. Again, note that the load connection precludes the flow of zero sequence components of the current to the load.

Analysis and Realization

In this dissertation a generalized passive bilateral compensator, capable of providing zero sequence compensation in addition to the conventional negative sequence and reactive power compensation, is derived.

A fundamental approach

Consider a generalized grounded three phase load (Fig.2-7) connected to a system with symmetrical line to neutral voltages $V_a = V$, $V_b = \alpha^2 V$ and $V_c = \alpha V$ (with the complexoperator $\alpha = e^{j120°}$). For convenience, the loads have

been represented by their complex admittances.

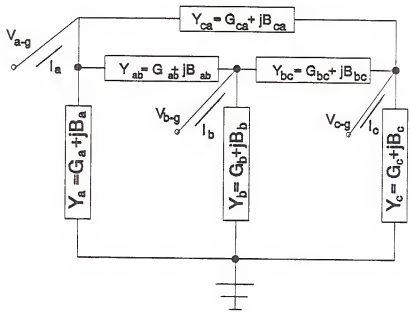

Figure 2-7. New generalized compensator. An admittance representation.

The compensating elements can be obtained by analyzing each equivalent single phase load separately. Their reactive components are compensated first and their remaining real parts effectively balanced through reactive compensation. The desired compensation for the complete grounded wye load is obtained by the superposition of all the previously derived compensators for each the equivalents single phase loads when considered separately. Starting with phase A, define its equivalent single phase load as formed by the admittances of the A-B and the A-Ground branches. After compensation of its reactive components by susceptances of the same magnitude and

opposite sign, the reduced equivalent circuit is

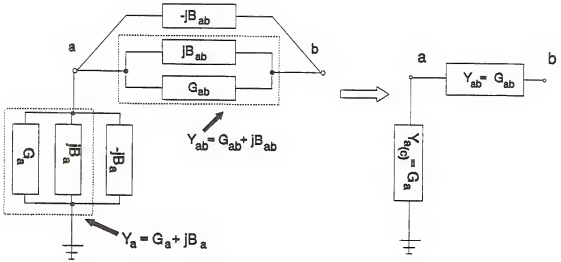

Figure 2-8. Reactive compensation of load susceptances of branches Y_{ab} and Y_a.

As a second step, the real admittance elements, G_a and G_{ab} are compensated with a reactive admittance network so as to obtain a balanced real power load.

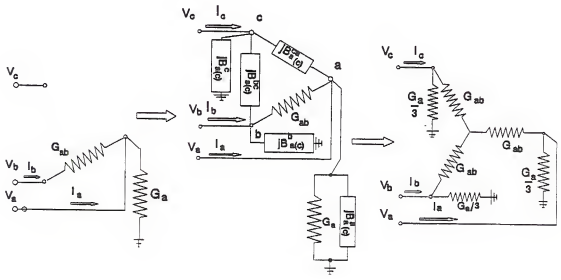

Figure 2-9. Reactive compensation and balanced equivalence of the branches A-B and A-ground conductances.

Sufficient conditions to achieve this goal are enforced by the following equations

$$Im[I_{a_{(c)}}] = 0$$

$$Re[I_{a_{(c)}}] = \frac{1\phi_{realpower}}{3} \tag{2-14}$$

From Fig.2-9, we can easily obtain the compensated line A current

$$I_{a_{(c)}} = V_a[G_a + jB^a_{a_{(c)}}] + V_{ab}G_{ab} + V_{ac}[jB^{ca}_{a_{(c)}}] \tag{2-15}$$

satisfying the requirement on the imaginary part, as indicated in (2-14)

$$Im[I^a_{a_{(c)}}] = VB^a_{a_{(c)}} + Im[\sqrt{3}\,VG_{ab}e^{j30^\circ}] + Im[\sqrt{3}\,VB^{ca}_{a_{(c)}}e^{60^\circ}] = 0 \tag{2-16}$$

and dividing through by V

$$B^a_{a_{(c)}} + \frac{\sqrt{3}}{2}G_{ab} + \frac{3}{2}B^{ca}_{a_{(c)}} = 0 \tag{2-17}$$

the real power requirement is satisfied when

$$(V)\,Re[I^a_{a_{(c)}}] = V[VG_a + \sqrt{3}\,VG_{ab}Cos30^\circ + \sqrt{3}\,VB^{ca}_{a_{(c)}}Cos60^\circ] = \frac{1\phi_{realpow}}{3} \tag{2-18}$$

where the single phase real power corresponding to the equivalent single phase load of phase A, is given by

$$1\phi_{realpower} = V^2[G_a + 3G_{ab}] \tag{2-19}$$

substituting in the previous equation

$$G_a + \frac{3}{2} G_{ab} + \frac{\sqrt{3}}{2} B^{ca}_{a(c)} = \frac{G_a}{3} + G_{ab} \tag{2-20}$$

solving for the unknown variable

$$B^{ca}_{a(c)} = -\frac{2}{\sqrt{3}} \left[\frac{2}{3} G_a + \frac{G_{ab}}{2}\right] \tag{2-21}$$

which when substituted back into (2-17) determines the value of the phase to ground compensating element

$$\begin{aligned} B^{a}_{a(c)} &= \frac{3}{\sqrt{3}} \left[\frac{2}{3} G_a + \frac{G_{ab}}{2}\right] - \frac{\sqrt{3}}{2} G_{ab} \\ &= \frac{2}{\sqrt{3}} G_a \end{aligned} \tag{2-22}$$

Still referring to Fig. 2-9, we now write the equation for the phase B line current

$$I^{b}_{a(c)} = V_b [jB^{b}_{a(c)}] + V_{ba} G_{ab} + V_{bc} [jB^{bc}_{a(c)}] \tag{2-23}$$

and multiplying through by the complex operator α, for convenience in determining its in phase and quadrature components

$$\alpha I^{b}_{a(c)} = j V B^{b}_{a(c)} + \sqrt{3}\, V G_{ab} e^{-j30^\circ} + \sqrt{3}\, V B^{bc}_{a(c)} e^{j120^\circ} = 0 \tag{2-24}$$

setting the imaginary part to zero

$$Im[\alpha I^{b}_{a_{(c)}}] = 0$$

$$\Rightarrow VB^{b}_{a_{(c)}} - \frac{\sqrt{3}}{2} VG_{ab} + \frac{3}{2} VB^{bc}_{a_{(c)}} = 0$$

(2-25)

dividing through by V and solving for the phase to ground element

$$B^{b}_{a_{(c)}} = \frac{\sqrt{3}}{2} G_{ab} - \frac{3}{2} B^{bc}_{a_{(c)}}$$

(2-26)

a third of the real power demand of the equivalent single phase load at phase A, requires that

$$\frac{RealPower^{b}_{a_{(c)}}}{3} = V^2 [\frac{G_a}{3} + G_{ab}]$$

$$= VRe[\alpha I^{b}_{a_{(c)}}]$$

(2-27)

where the real part of the compensated phase B current is

$$Re[\alpha I^{b}_{a_{(c)}}] = \frac{3}{2} VG_{ab} - \frac{\sqrt{3}}{2} VB^{bc}_{a_{(c)}}$$

(2-28)

which together with the previous equation give

$$\frac{3}{2} G_{ab} - \frac{\sqrt{3}}{2} B^{bc}_{a_{(c)}} = \frac{G_a}{3} + G_{ab}$$

$$\Rightarrow B^{bc}_{a_{(c)}} = \frac{G_{ab}}{\sqrt{3}} - \frac{2}{3\sqrt{3}} G_a$$

(2-29)

and back substituting in (2-26) solves for the corresponding phase to ground element.

$$B^{b}_{a_{(c)}} = \frac{G_a}{\sqrt{3}}$$

(2-30)

Similarly, the line C current contribution for the equivalent single phase A compensation can be obtained from Fig.2-9

$$I^{c}_{a_{(c)}} = V_c(jB^{c}_{a_{(c)}}) + V_{ca}(jB^{ca}_{a_{(c)}}) + V_{cb}(jB^{bc}_{a_{(c)}})$$

(2-31)

and rotating by the complex operator α^2 for ease in determining its in phase and quadrature components

$$\alpha^2 I^{c}_{a_{(c)}} = V(jB^{c}_{a_{(c)}}) + \sqrt{3}\,VB^{ca}_{a_{(c)}} e^{j120^\circ} + \sqrt{3}\,VB^{bc}_{a_{(c)}} e^{j60^\circ}$$

(2-32)

where the requirement on the imaginary component is

$$Im[\alpha^2 I^{c}_{a_{(c)}}] = VB^{c}_{a_{(c)}} + \frac{3}{2}VB^{ca}_{a_{(c)}} + \frac{3}{2}VB^{bc}_{a_{(c)}} = 0$$

(2-33)

dividing through by V and substituting for $B_{(a)c}{}^{ca}$ and $B_{(a)c}{}^{bc}$, the phase C to ground element of the compensator for the equivalent single phase A circuit is obtained.

$$B^{c}_{a_{(c)}} - \sqrt{3}\left(\frac{2}{3}G_a + \frac{G_{ab}}{2}\right) + \frac{3}{2}\left(\frac{G_{ab}}{\sqrt{3}} - \frac{2}{3\sqrt{3}}G_a\right) = 0$$

$$B^{c}_{a_{(c)}} = \sqrt{3}\,G_a$$

(2-34)

It is seen that the remaining compensating condition on the real power supplied by phase C is automatically satisfied.

$$
\begin{aligned}
V(Re[\alpha^2 I^{c}_{a_{(c)}}]) &= V(-\frac{\sqrt{3}}{2} VB^{ca}_{a_{(c)}} + \frac{\sqrt{3}}{2} VB^{bc}_{a_{(c)}} \\
&= V^2 [-\frac{\sqrt{3}}{2} (-\frac{2}{\sqrt{3}}) (\frac{2}{3} G_a + \frac{G_{ab}}{2}) + \frac{\sqrt{3}}{2} (\frac{G_{ab}}{\sqrt{3}} - \frac{2}{3\sqrt{3}} G_a) \\
&= V^2 (\frac{G_a}{3} + G_{ab}) \\
&= \frac{RealPower_{a(c)}}{3}
\end{aligned}
$$

(2-35)

Proceeding in the same manner, after compensating for the load susceptances B_{bc}, B_{ca}, B_b and B_c, it is possible to separately obtain the compensating elements for the equivalent phase B and C single phase loads. The required compensation for the phase B equivalent is determined to be

$$
\begin{aligned}
B^{a}_{b_{(c)}} &= \sqrt{3} G_b & B^{ab}_{b_{(c)}} &= -\frac{G_{bc}}{\sqrt{3}} - \frac{4}{3\sqrt{3}} G_b \\
B^{b}_{b_{(c)}} &= \frac{2}{\sqrt{3}} G_b & B^{ca}_{b_{(c)}} &= \frac{G_{bc}}{\sqrt{3}} - \frac{2}{3\sqrt{3}} G_b \\
B^{c}_{b_{(c)}} &= \frac{G_b}{\sqrt{3}}
\end{aligned}
$$

(2-36)

and for the single phase C equivalent circuit

$$
\begin{aligned}
B^{a}_{c_{(c)}} &= \frac{G_c}{\sqrt{3}} & B^{ab}_{c_{(c)}} &= \frac{G_{ca}}{\sqrt{3}} - \frac{2}{3\sqrt{3}} G_c \\
B^{b}_{c_{(c)}} &= \sqrt{3} G_c & B^{bc}_{c_{(c)}} &= -\frac{4}{3\sqrt{3}} G_c - \frac{G_{ca}}{\sqrt{3}} \\
B^{c}_{c_{(c)}} &= \frac{2}{\sqrt{3}} G_c
\end{aligned}
$$

(2-37)

These values are reduced to the compensating elements for the delta or ungrounded load arrangement by setting G_a,G_b and G_c, the phase to ground load admittances, equal to zero.
The corresponding compensating circuits with their respective balanced equivalent admittance networks are shown in Fig.2-10 and 2-11 below

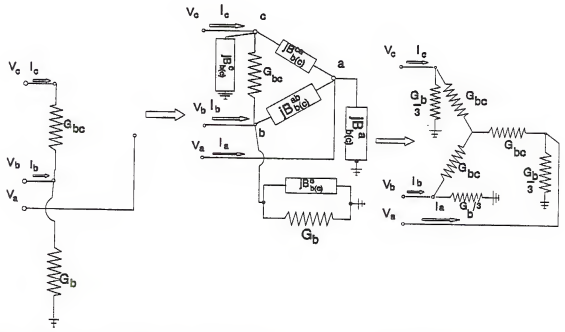

Figure 2-10. Reactive compensation and balanced equivalence of the branches B-C and B-ground conductances.

Complete compensation of the three phase grounded load is obtained by adding the compensating susceptances, in each branch, determined separately from the single phase equivalents. Figure 2-12 shows the compensating and three phase balanced admittance equivalent network.

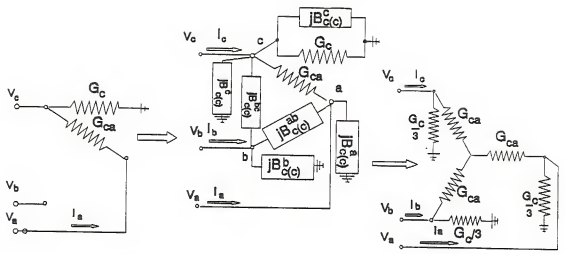

Figure 2-11. Reactive compensation and balanced equivalence of the branches C-A and C-ground conductances.

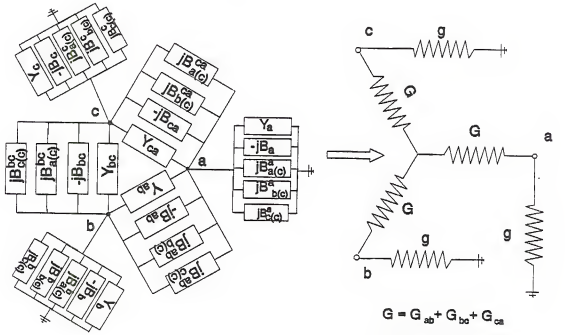

Figure 2-12. Complete reactive compensator for an unbalanced three phase grounded load.

A symmetrical sequence solution

Consider an equivalent compensator, connected to a balanced three phase grounded source with the general configuration shown in Fig.2-7. This is the most general representation of a four terminal element (counting ground as a terminal), since it contains all possible interconnections between its terminals. The Y's represent the equivalent admittance values of its elements. Assuming balanced positive sequence rotation of the source voltages

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 \\ \alpha^2 \\ \alpha \end{bmatrix} V \qquad (2\text{-}38)$$

The currents supplied by the compensator when connected to the equivalent system are

$$\begin{aligned} -I_{a_{(c)}} &= (V_a - V_b)\, Y_{ab} + (V_a - V_c)\, Y_{ca} + V_a Y_a \\ &= Y_{ab}(1-\alpha^2)\, V + Y_{ca}(1-\alpha)\, V + Y_a V \\ -I_{b_{(c)}} &= (V_b - V_c)\, Y_{bc} + (V_b - V_a)\, Y_{ab} + V_b Y_b \\ &= Y_{bc}(\alpha^2 - \alpha)\, V + Y_{ab}(\alpha^2 - 1) + Y_b \alpha^2 V \\ -I_{c_{(c)}} &= (V_b - V_c)\, Y_{bc} + (V_c - V_a)\, Y_{ca} + V_c Y_c \\ &= Y_{bc}(\alpha - \alpha^2)\, V + Y_{ca}(\alpha - 1) + \alpha Y_c V \end{aligned} \qquad (2\text{-}39)$$

The sequence components of the current can be obtained from the phase quantities by

$$\begin{pmatrix} I_0 \\ I_+ \\ I_- \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{pmatrix}\begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix} \tag{2-40}$$

and substituting for the compensator currents

$$\begin{aligned} -I_{a_0} &= -\frac{1}{3}\left(I_{a_{(c)}} + I_{b_{(c)}} + I_{c_{(c)}}\right) \\ &= \frac{1}{3}\left(Y_a + \alpha^2 Y_b + \alpha Y_c\right) V \\ -I_{a_+} &= -\frac{1}{3}\left(I_{a_{(c)}} + \alpha I_{b_{(c)}} + \alpha^2 I_{c_{(c)}}\right) \\ &= \left[Y_{ab} + Y_{bc} + Y_{ca} + \frac{1}{3}\left(Y_a + Y_b + Y_c\right)\right] V \\ -I_{a_-} &= -\frac{1}{3}\left(I_{a_{(c)}} + \alpha^2 I_{b_{(c)}} + \alpha I_{c_{(c)}}\right) \\ &= -\left[\alpha^2 Y_{ab} + Y_{bc} + \alpha Y_{ca} - \frac{1}{3}\left(Y_a + \alpha Y_b + \alpha^2 Y_c\right)\right] \end{aligned} \tag{2-41}$$

where the negative sign refers to the sequence components of the current flowing out of the compensator into the system. By restricting ourselves to a passive reactive compensator, that is, one made up of capacitive and inductive elements, only the imaginary component of the compensator admittances need to be considered (ie the susceptance B, Y = G + jB)

$$-I_{a_0} = \frac{1}{3} j\,(B_a + \alpha^2 B_b + \alpha B_c)\,V$$

$$-I_{a_+} = j\,(B_{ab} + B_{bc} + B_{ca} + \frac{1}{3}(B_a + B_b + B_c))$$

$$-I_{a_-} = -j\,(\alpha^2 B_{ab} + B_{bc} + \alpha B_{ca} - \frac{1}{3}(B_a + \alpha B_b + \alpha^2 B_c))\,V$$

(2-42)

From which expressions for the real and imaginary parts of the sequence currents may be obtained

$$\frac{1}{2\sqrt{3}} B_b V - \frac{1}{2\sqrt{3}} B_c V = -\,Re[I_{a_0}]$$

$$\frac{1}{3} B_a V - \frac{1}{6} B_b V - \frac{1}{6} B_c V = -Im[I_{a_0}]$$

$$\frac{1}{3} B_a V + \frac{1}{3} B_b V + \frac{1}{3} B_c V + B_{ab} + B_{bc} + B_{ca} = -Im[I_{a_+}]$$

$$-\frac{1}{2\sqrt{3}} B_b V + \frac{1}{2\sqrt{3}} B_c V - \frac{\sqrt{3}}{2} B_{ab} V + \frac{\sqrt{3}}{2} B_{ca} V = -Re[I_{a_-}]$$

$$\frac{1}{3} B_a V - \frac{1}{6} B_b V - \frac{1}{6} B_c V + \frac{1}{2} B_{ab} V - B_{bc} V + \frac{1}{2} B_{ca} V = -Im[I_{a_-}]$$

(2-43)

and in matrix notation

$$\begin{pmatrix} 0 & \frac{1}{2}\sqrt{3} & -\frac{1}{2}\sqrt{3} & 0 & 0 & 0 \\ \frac{1}{3} & -\frac{1}{6} & -\frac{1}{6} & 0 & 0 & 0 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 1 & 1 & 1 \\ 0 & -\frac{1}{2}\sqrt{3} & \frac{1}{2}\sqrt{3} & -\frac{\sqrt{3}}{2} & 0 & \frac{\sqrt{3}}{2} \\ \frac{1}{3} & -\frac{1}{6} & -\frac{1}{6} & \frac{1}{2} & -1 & \frac{1}{2} \end{pmatrix} \begin{pmatrix} B_a \\ B_b \\ B_c \\ B_{ab} \\ B_{bc} \\ B_{ca} \end{pmatrix} = -\frac{1}{V} \begin{pmatrix} Re[I_{a_0}] \\ Im[I_{a_0}] \\ Im[I_{a_+}] \\ Re[I_a-] \\ Im[I_{a_-}] \end{pmatrix}$$

(2-44)

of the form

$$[A]\underline{b} = -(\frac{1}{V})\,\underline{i} \tag{2-45}$$

a linear system of five equations and six unknowns also known as an undetermined system with infinitely many solutions. Provided the rank of [A] is equal to the number of equations, it is possible to obtain the minimum norm solution for $\underline{b}$ by premultiplying $\underline{i}$ by the Moore-Penrose inverse of [A], $[A]^{+}$.

$$[A^{+}] = [A]^{*}[AA^{*}]^{-1} \tag{2-46}$$

$$\underline{b}_{min} = (-\frac{1}{V})\,[A^{+}]\,\underline{i} \tag{2-47}$$

where $\underline{b}_{min}$ represents the minimum norm susceptance vector. It is possible to relate the susceptance vector to the vector of the reactive power rating of the different compensator elements

$$\underline{MVAR} = \begin{pmatrix} MVAR_a \\ MVAR_b \\ MVAR_c \\ MVAR_{ab} \\ MVAR_{bc} \\ MVAR_{ca} \end{pmatrix} = V^2 \begin{pmatrix} B_a \\ B_b \\ B_c \\ 3\,B_{ab} \\ 3\,B_{bc} \\ 3\,B_{ca} \end{pmatrix} = V^2\,[D]\,\underline{b} \tag{2-48}$$

solving for the susceptance vector $\underline{b}$

$$\underline{b} = \left(\frac{1}{V^2}\right) [D]^{-1} \underline{MVAR} \tag{2-49}$$

and replacing in the original (2-45)

$$[A]\,\underline{b} = \left(\frac{1}{V^2}\right) [A]\,[D]^{-1} \underline{MVAR} = \left(-\frac{1}{V}\right) \underline{i} \tag{2-50}$$

$$[H]\,\underline{MVAR} = -V\underline{i} \tag{2-51}$$

where

$$[H] = [A]\,[D]^{-1} \tag{2-52}$$

and proceeding as before, taking the Moore-Penrose inverse of [H]

$$[H]^{+} = [H]^{*}\,[HH^{*}]^{-1} \tag{2-53}$$

we can solve for our desired result

$$\underline{MVAR}_{min} = V[H]^{+}\underline{i} \tag{2-54}$$

which conforms with the minimum norm MVAR solution, that is, the minimum agregated MVAR capacity compensator that will produce the required compensation.

CHAPTER 3
STEADY STATE ANALYSIS

System Model

In order to evaluate the feasibility of the results, the parameters which have been used in our computations correspond to those of a 500 KV system [7]. The basic steady state model used in the following analysis comprises two ideal sources interconnected by a transmission line through step up transformers.

The electro-mechanical interactions of a real machine, when subjected to the disturbances associated with the sudden insertion of the sequence compensator proposed in this dissertation, will be studied in more detail in the following chapter.

The values used for our system parameters in the basic model, (Fig.3-1) in per unit on a 500 KV voltage base and 1000 MVA base are shown in table 3-1.

Table 3-1. Steady state model impedance values.

	Z_s	Z_r	Z_{cs}	Z_{cr}	Z_l	Z_c
Positive Sequence	0.002355 j0.04541	0.01632 j0.4781	-j16.7567	-j58.6493	0.01454 j0.21186	-j11.72539
Zero Sequence	0.03311 j0.09889	0.1096 j0.4335	-j30	-j100	0.20356 j0.66424	-j14.96

Where Z_s and Z_r stand for the sending and receiving ends equivalent source impedances; Z_{cs}, Z_{cr} for the equivalent bus capacitive reactances at the sending and receiving buses and Z_l, Z_c the series impedance and the charging reactance of the equivalent line pi model.

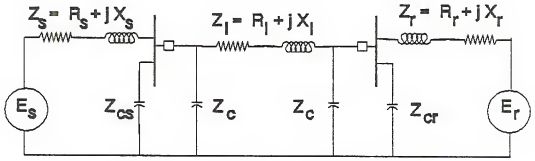

Fig.3-1. Single line diagram of basic model.

Unless otherwise specified, the single pole opening (SPO) is always assumed to occur in phase a. This simplifies the analysis and produces, after some manipulation, results equally valid for the other two phases. It is assumed that the line can be adequately represented by its sequence impedances; the degree of transposition being such that symmetrical sequence analysis is possible. The capacitive reactances at the bus terminals relate to those associated with the other lines out of these buses. It is specified here to account for the general case when it is not part of the equivalent source impedances.

General Approach

The single pole opening condition in a transmission line can be represented in symmetrical sequence components, as the parallel interconnection of 2-port sequence networks, in such a way that the boundary conditions pertaining to the referred unbalance are satisfied.

Assuming transposition of the affected line, the symmetrical components transformation by virtue of its decoupling properties, allows us to analyze each sequence network separately. Equivalently, voltages and currents in the physical network may be viewed as composed of a pre-unbalance (or pre-fault) term plus other perturbation quantities.
A one line representation of our network model is presented in Fig.3-2. This figure also shows the pre-fault terminal line voltages and currents and their change, in terms of their symmetrical sequence composition during a phase A open pole condition. Each sequence network may be analyzed independently of each other due to the decoupling effect produced by the symmetrical sequence transformation.

By eliminating or shunting out the flow of ΔI^{-} and ΔI^{0}, (the change in negative and zero sequence components of the current), into the sending and receiving end systems two of

our major objectives are achieved:

1) Prevention of the flow of the undesired sequence components of the line current into the remote systems. Voltage unbalances are simultaneously eliminated.
2) Continuous operation under the SPO (single pole opening) condition without jeopardizing the integrity of the system.

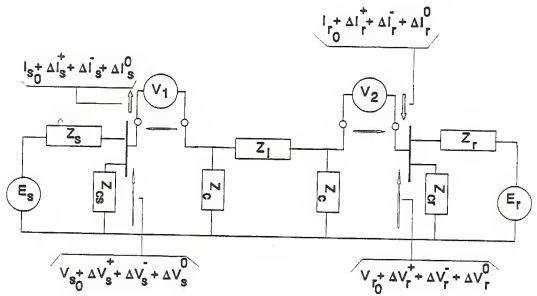

Fig.3-2. Equivalent one-line representation with pre-fault and change quantities. Phase A SPO.

Negative and zero sequence current compensation is obtained by means of inserting an unbalanced reactive load of "appropriate size" at the bus terminals of the affected line during the unbalanced condition. These loads are also referred to as selective sequence current filters or compensators

throughout this dissertation. These compensators present a low impedance path to the flow of negative and zero sequence currents, and are, in effect, negative and zero sequence current filters. By appropriate injection of negative and zero sequence currents, at the bus terminals of the line, it is possible to restrict the flow of said currents, in a closed loop, around the compensators and the affected line. In this manner, the ill effects of negative and zero sequence current flow and distribution, throughout the remote sending and receiving systems, are avoided. Furthermore, negative and zero sequence current compensation enhances the power transfer capacity under the open pole condition and allows for indefinite time operation in two phases (restricted only by the thermal rating of the compensator itself and the line conductor) in either a grounded or an ungrounded system.

Due to the inherent decoupling property of the symmetrical components transformation on the type of elements considered here, voltage drops in a given sequence are associated only to the flow of the same sequence current component. Thus, positive, negative and zero sequence (in a grounded system) voltage changes are caused by the flow of positive, negative and zero sequence currents respectively. Figures 3-3 through 3-5 show the change quantities generated by the SPO condition in the sequence networks. Possible corrective measures to lessen the undesired effects associated with this unbalance can be inferred from these circuits.

Furthermore, by reactive compensation of the positive sequence network, the power transfer capacity through the affected line may be sufficiently increased after pole opening as to nullify the reduction in power transfer that would normally occur during this condition. The compensators are active only during the SPO interval.

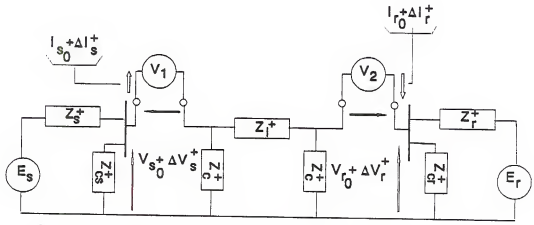

Fig.3-3. Positive sequence network of basic model during SPO condition.

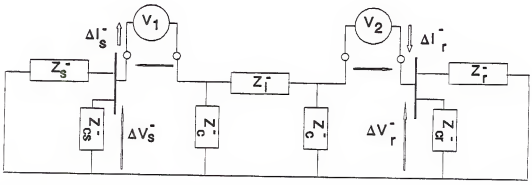

Fig.3-4. Negative sequence network of basic model during SPO condition.

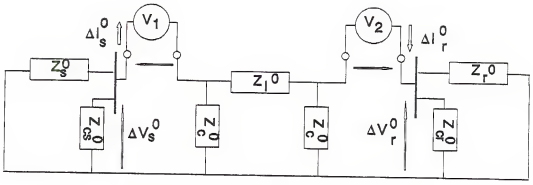

Fig.3-5. Zero sequence network of basic model during SPO condition.

Ungrounded System

In order to simplify the analysis and to illustrate the application of this new concept we will begin by studying the effects of negative sequence compensation during the single pole opening condition in an ungrounded system.

SPO Analysis

Assuming phase A is open, the interconnections between the sequence networks must satisfy the restrictions imposed by the unbalance condition. The sequence voltages at the terminals associated with the opening condition are equal,

$$V_1 = V_1^+ = V_1^-$$
$$V_2 = V_2^+ = V_2^- \qquad (3\text{-}1)$$

which satisfies the zero voltage requirement of the healthy phases across the associated series fault terminals at the sending and receiving end

$$V_{a1} = 3\,V_1 \qquad V_{a2} = 3\,V_2$$
$$V_{b1} = 0 \qquad V_{b2} = 0$$
$$V_{c1} = 0 \qquad V_{c2} = 0$$

(3-2)

The current at the opening terminal in the sending and receiving end satisfies

$$\begin{pmatrix} I_{as} \\ I_{ar} \end{pmatrix} = \begin{pmatrix} I_{s(0)} \\ I_{r(0)} \end{pmatrix} + \begin{pmatrix} \Delta I_s^+ \\ \Delta I_r^+ \end{pmatrix} + \begin{pmatrix} \Delta I_s^- \\ \Delta I_r^- \end{pmatrix} = \underline{0}$$

(3-3)

as seen in the superposition of the currents shown in Fig.3-3 and 3-4.

It is possible to express the positive and negative sequence delta currents at the sending and receiving ends of the line in terms of the port voltages V_1 and V_2

$$\begin{pmatrix} -\Delta I_s^+ \\ \Delta I_r^+ \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix}_+ \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = (Z)_+^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}$$

(3-4)

$$\begin{pmatrix} -\Delta I_s^- \\ \Delta I_r^- \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix}_- \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = (Z)_-^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}$$

(3-5)

where $(Z)_+$ and $(Z)_-$ are the two-port impedance matrices of the positive and negative sequence networks as seen from the unbalance terminals.

Substituting (3-4) and (3-5) into (3-3), a matrix equation of the following form is obtained

$$(A_0)\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \underline{b}_0 \qquad (3\text{-}6)$$

from which the port voltages are easily found and the sequence networks completely solved.

For this condition, a single pole opening at each of the line terminals, the negative sequence components of the currents at the sending and receiving terminals of the line do flow into the remote systems. The generated unbalances prevent permanent operation of the line under normal SPO.

Negative Sequence Compensation

Negative sequence compensation will prevent the flow of unbalanced currents, originated during the open pole condition, into the remote systems. This provides for permanent operation of the line in two phases. The determination of the compensating currents, required to accomplish our objective, may be seen from the associated sequence networks when considered separately, Fig.3-3 and 3-6.

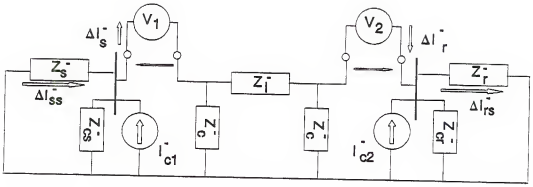

Fig.3-6. Ungrounded case. Compensated negative sequence network under SPO.

The SPO condition requires the phase current at the open terminals to equal zero. Permanent operation in two phases is feasible if the amount of negative sequence current, generated by the open pole condition and flowing into the remote systems, is reduced to acceptable levels.

Referring to Fig.3-6, ideally we will require

$$\begin{pmatrix} \Delta I_{ss}^- \\ \Delta I_{rs}^- \end{pmatrix} = \underline{0} \tag{3-7}$$

Two-port theory allows us to immediately obtain the expressions associated with the change in voltage and current in the positive sequence network

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = (Z)_+ \begin{pmatrix} -\Delta I_s^+ \\ \Delta I_r^+ \end{pmatrix} \tag{3-8}$$

$$\begin{pmatrix} -\Delta I_s^+ \\ \Delta I_r^+ \end{pmatrix} = (Z)_+^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{3-9}$$

$$\begin{pmatrix} \Delta I_s^+ \\ \Delta I_r^+ \end{pmatrix} = (U)(Z)_+^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}$$

$$\textit{where} \qquad (U) = \begin{pmatrix} -1 & 0 \\ 0 & 1 \end{pmatrix} \tag{3-10}$$

The negative sequence network can be analyzed by superimposing the contributions of its equivalent voltage and current sources acting separately (Fig.3-6). Thereby, accounting for the effects of the SPO condition and that of the compensating network,

$$\begin{pmatrix} \Delta I_s^- \\ \Delta I_r^- \end{pmatrix} = (U)(Z)_-^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (K_1)_- \begin{pmatrix} I_{c1}^- \\ I_{c2}^- \end{pmatrix} \tag{3-11}$$

$$\begin{pmatrix} \Delta I_{ss}^- \\ \Delta I_{rs}^- \end{pmatrix} = (U)(Z)_-^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (K_2)_- \begin{pmatrix} I_{c1}^- \\ I_{c2}^- \end{pmatrix} \tag{3-12}$$

where (K_1). and (K_2). are current distribution matrices. Substituting (3-10),(3-11) and (3-12) into (3-3) and (3-7), after regrouping terms we obtain,

$$\begin{pmatrix} 2\,(U)\,(Z)^{-1} & (K_1) \\ (U)\,(Z)^{-1} & (K_2) \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \\ I_{c1}^{-} \\ I_{c2}^{-} \end{pmatrix} = \begin{pmatrix} -I_{s(0)} \\ -I_{r(0)} \\ 0 \\ 0 \end{pmatrix} \tag{3-13}$$

which is of the form

$$(A_1) \begin{pmatrix} V_1 \\ V_2 \\ I_{c1}^{-} \\ I_{c2}^{-} \end{pmatrix} = \underline{b}_1 \tag{3-14}$$

The compensating currents I_{c1}^{-} and I_{c2}^{-} can now be used to determine the required impedances of the negative sequence filter.

It has been shown that by adequately compensating the negative sequence currents, it is possible to operate a delta or ungrounded three phase line with only two conductors without incurring into unacceptable operating unbalances.

Simplified Analysis

The compensator presents a preferred path to the flow of negative sequence current during the SPO condition. This in effect, is equivalent to substituting the compensating current sources in the respective sequence network, Fig.3-6, by a short circuit connection as indicated next in Fig.3-7.

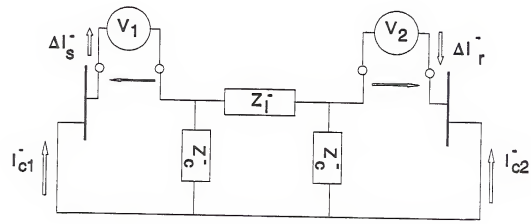

Fig.3-7. Reduced negative sequence network under SPO conditions.

The change in current in the positive sequence network, remains as previously determined (3-10). The change in negative sequence current can now be written from Fig.3-7

$$\begin{pmatrix} \Delta I_s^- \\ \Delta I_r^- \end{pmatrix} = (\bar{Z}_{-})^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \qquad (3\text{-}15)$$

and the compensating currents correspond to

$$\begin{pmatrix} \bar{I}_{c1} \\ \bar{I}_{c2} \end{pmatrix} = \begin{pmatrix} \Delta \bar{I}_s \\ -\Delta \bar{I}_r \end{pmatrix}$$

(3-16)

where $(\bar{Z}_+)$ is now the two-port impedance matrix as seen from each pair of open pole terminals when the source impedances are shorted out. Substituting (3-10) and (3-15) into (3-3) and rearranging, a standard linear equation is obtained

$$(\underline{A}_2)\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \underline{b}_2$$

(3-17)

The compensating currents I_{c1} and I_{c2} are readily determined by back substitution.

Positive Sequence Reactive Compensation

To determine the effect of increasing the positive sequence reactive compensation during the SPO condition, reactive generation at the busbar terminals is incorporated into the model.

By restricting ourselves to reactive power generation, this compensation can be modeled by a passive element (ie, a shunt capacitor bank at each bus terminal) easily incorporated in our generalized compensator. The representation of this element in the negative and zero sequence networks should be omitted due to the effective short circuit at the bus terminals caused by the respective sequence compensators. As shown in the derivation that follows, it is possible to

express the positive sequence reactive current injections in terms of the equivalent voltage sources (V_1, V_2) representing the unbalance condition. Current changes in the positive sequence network, due to positive sequence reactive compensation, can be separately determined by superposition. The corresponding compensating current sources, I_{c1}^+ and I_{c2}^+, flow into the sending and receiving bus terminals respectively while the voltage sources are shorted out.

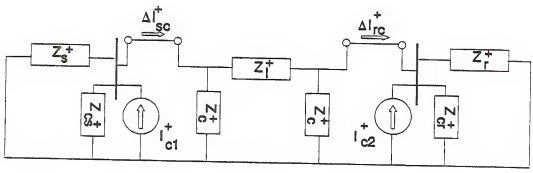

Fig.3-8. Positive sequence reactive compensation contribution during SPO conditions.

The total change in sending and receiving currents is now given by

$$\begin{pmatrix} \Delta I_{sT}^+ \\ \Delta I_{rT}^+ \end{pmatrix} = \begin{pmatrix} \Delta I_s^+ \\ \Delta I_r^+ \end{pmatrix} + \begin{pmatrix} \Delta I_{sc}^+ \\ \Delta I_{rc}^+ \end{pmatrix} \qquad (3\text{-}18)$$

where the extreme right hand term, is seen to be, from Fig.3-8

$$\begin{pmatrix} \Delta I_{sc}^{+} \\ \Delta I_{rc}^{+} \end{pmatrix} = (K)_{+} \begin{pmatrix} I_{c1}^{+} \\ I_{c2}^{+} \end{pmatrix}$$

(3-19)

and $(K)_{+}$ is a current distribution matrix. Substituting this last equation and (3-10) back into (3-18) results in,

$$\begin{pmatrix} \Delta I_{sT}^{+} \\ \Delta I_{rT}^{+} \end{pmatrix} = (U)(Z)_{+}^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (K)_{+} \begin{pmatrix} I_{c1}^{+} \\ I_{c2}^{+} \end{pmatrix}$$

(3-20)

and making use of the requirement that the compensating currents are generated by purely capacitive elements

$$\begin{pmatrix} I_{c1}^{+} \\ I_{c2}^{+} \end{pmatrix} = \begin{pmatrix} -jB_s & 0 \\ 0 & -jB_r \end{pmatrix} \begin{pmatrix} V_{sn}^{+} \\ V_{rn}^{+} \end{pmatrix}$$

(3-21)

where

$$\begin{pmatrix} V_{sn}^{+} \\ V_{rn}^{+} \end{pmatrix} = \begin{pmatrix} V_{s(0)} \\ V_{r(0)} \end{pmatrix} + \begin{pmatrix} \Delta V_s^{+} \\ \Delta V_r^{+} \end{pmatrix}$$

(3-22)

and

$$\begin{pmatrix} \Delta V_s^{+} \\ \Delta V_r^{+} \end{pmatrix} = (Z_s)_{+} \begin{pmatrix} \Delta I_{sT}^{+} \\ \Delta I_{rT}^{+} \end{pmatrix}$$

(3-23)

$(Z_s)_+$ is the equivalent positive sequence source impedance matrix. After substituting (3-20) into this last equation, we obtain

$$\begin{pmatrix} \Delta V_s^+ \\ \Delta V_r^+ \end{pmatrix} = (Z_s)_+(U)(Z)_+^{-1}\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (Z_s)_+(K)_+\begin{pmatrix} I_{c1}^+ \\ I_{c2}^+ \end{pmatrix} \tag{3-24}$$

which when replaced into (3-22) and the result in turn into (3-21) yields

$$\begin{pmatrix} I_{c1}^+ \\ I_{c2}^+ \end{pmatrix} = -jB_c\left[\begin{matrix} V_{s(0)} \\ V_{r(0)} \end{matrix} + (Z_s)_+^{-1}(U)(Z)_+^{-1}\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (Z_s)(K)_+\begin{pmatrix} I_{c1}^+ \\ I_{c2}^+ \end{pmatrix}\right] \tag{3-25}$$

and solving for the compensating currents

$$\begin{pmatrix} I_{c1}^+ \\ I_{c2}^+ \end{pmatrix} = -jB_c\left[(I) + jB_c(Z_s)_+(K)\right]^{-1}\left[\begin{pmatrix} V_{s(0)} \\ V_{r(0)} \end{pmatrix} + (Z_s)_+(U)(Z)_+^{-1}\begin{pmatrix} V_1 \\ V_2 \end{pmatrix}\right] \tag{3-26}$$

where it has been assumed that the positive sequence compensating suceptance at the sending and receiving ends are equal

$$B_s = B_r = B_c \tag{3-27}$$

Substituting back into (3-19) and (3-18), which together with the negative sequence network (3-12) and (3-11), can be grouped together to satisfy the open pole and the selective compensator conditions, (3-3) and (3-7). An ordinary linear

equation is obtained

$$(A_2)\begin{pmatrix} V_1 \\ V_2 \\ I_{c1} \\ I_{c2} \end{pmatrix} = \underline{b}_2 \qquad (3\text{-}28)$$

which is easily solved for the desired unknowns.

Grounded System

A more general system configuration is now considered. The equivalent zero sequence impedance of the line is now connected to the equivalent zero sequence impedances of the remote sources through the ground path of the interconnecting transformers. This constitutes a more common arrangement inhigh voltage transmission systems, where the neutral terminal is solidly grounded.

SPO Analysis

To analyze the single pole opening condition (SPO) in a grounded system, the zero sequence network, in addition to the positive and negative sequence networks, must also be considered. That corresponding to our basic model is shown in Fig.3-5. Assuming that phase A is subject to a SPO condition at both terminals of the line, the sequence voltages at the terminals associated with the opening condition must be equal

$$V_1 = V_1^+ = V_1^- = V_1^0$$
$$V_2 = V_2^+ = V_2^- = V_2^0$$

(3-29)

which also satisfies (3-2), the zero voltage requirement of the healthy phases across the associated series fault terminals at the sending and receiving ends of the line. The phase A current, flowing through the open terminal in the sending and receiving end, must satisfy

$$\begin{pmatrix} I_{as} \\ I_{ar} \end{pmatrix} = \begin{pmatrix} I_{s(0)} \\ I_{r(0)} \end{pmatrix} + \begin{pmatrix} \Delta I_s^+ \\ \Delta I_r^+ \end{pmatrix} + \begin{pmatrix} \Delta I_s^- \\ \Delta I_r^- \end{pmatrix} + \begin{pmatrix} \Delta I_s^0 \\ \Delta I_r^0 \end{pmatrix} = \underline{0}$$

(3-30)

which has been obtained by the superposition of the corresponding sequence currents flowing through the equivalent terminals representing the open pole condition and shown separately in Fig.3-3,3-4 and 3-5.

The zero sequence currents, at the sending and receiving ends of the line, can be expressed in terms of the port voltages V_1 and V_2

$$\begin{pmatrix} -\Delta I_s^0 \\ \Delta I_r^0 \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix}_0 \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = (Z)_0^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}$$

(3-31)

where $(Z)_0$ is the two-port impedance matrix of the zero sequence network as seen from the open pole terminals. Substituting (3-5), (3-10) and (3-31) into (3-30) a matrix equation similar in form to (3-6) is obtained. The port

voltages may then be obtained and the sequence networks completely solved.

Zero Sequence Compensation

The zero sequence network of our model system during the SPO condition and zero sequence current compensation is shown in Fig.3-9.

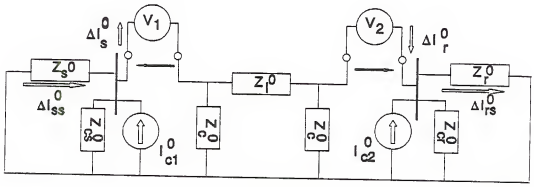

Fig.3-9. Compensated zero sequence network under SPO.

The positive and negative sequence networks are similar to those of Fig.3-3 and 3-6. The conditions imposed by the series faults on the phase A currents, at the remote terminals of the line, must satisfy (3-30) and the requirements on the flow of unbalanced currents into the remote systems

$$\begin{pmatrix} \Delta I_{ss}^- \\ \Delta I_{rs}^- \end{pmatrix} = 0 \qquad \begin{pmatrix} \Delta I_{ss}^0 \\ \Delta I_{rs}^0 \end{pmatrix} = 0 \tag{3-32}$$

Decoupling of the sequence networks assures the validity of previous equations (3-10 through 3-12), which are repeated

here for clarity

$$\begin{pmatrix} \Delta I_s^+ \\ \Delta I_r^+ \end{pmatrix} = (U)(Z)_+^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{3-33}$$

$$\begin{pmatrix} \Delta I_s^- \\ \Delta I_r^- \end{pmatrix} = (U)(Z)_-^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (K_1)_- \begin{pmatrix} I_{c1}^- \\ I_{c2}^- \end{pmatrix} \tag{3-34}$$

$$\begin{pmatrix} \Delta I_{ss}^- \\ \Delta I_{rs}^- \end{pmatrix} = (U)(Z)_-^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (K_2)_- \begin{pmatrix} I_{c1}^- \\ I_{c2}^- \end{pmatrix} = \underline{0} \tag{3-35}$$

The change in currents ΔI_s^0 and ΔI_r^0 may be obtained by superimposing the effects of the voltage and current sources separately. When determining the contributions due to the voltage sources, the current sources are open circuited and when computing those of the current sources the voltage sources are short circuited. Proceeding as described, the change in currents in the zero sequence network can be shown to be

$$\begin{pmatrix} \Delta I_s^0 \\ \Delta I_r^0 \end{pmatrix} = (U)(Z)_0^{-1} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (K_3)_0 \begin{pmatrix} I_{c1}^0 \\ I_{c2}^0 \end{pmatrix} = \underline{0} \tag{3-36}$$

where $(Z)_0$ is the two port zero sequence impedance matrix, as seen from the unbalanced terminals, and $(K_3)_0$ is a current distribution matrix.

Substituting (3-33), (3-34) and (3-36) into (3-30)

$$\begin{pmatrix} I_s^0 \\ I_r^0 \end{pmatrix} + (U)(Z)_+^{-1}\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (U)(Z)_-^{-1}\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (K_1)_-\begin{pmatrix} I_{c1}^- \\ I_{c2}^- \end{pmatrix} + (U)(Z)_0^{-1}\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (K_3)_0\begin{pmatrix} I_{c1}^0 \\ I_{c2}^0 \end{pmatrix} = \underline{0} \tag{3-37}$$

and reordering terms

$$(U)\left[(Z)_+^{-1} + (Z)_-^{-1} + (Z)_0^{-1}\right]\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (K_1)_-\begin{pmatrix} I_{c1}^- \\ I_{c2}^- \end{pmatrix} + (K_3)_0\begin{pmatrix} I_{c1}^0 \\ I_{c2}^0 \end{pmatrix} = -\begin{pmatrix} I_{s(0)} \\ I_{r(0)} \end{pmatrix} \tag{6-38}$$

which together with (3-35) and the restriction of zero current flow into the remote systems (Fig.3-9)

$$\begin{pmatrix} \Delta I_{ss}^0 \\ \Delta I_{rs}^0 \end{pmatrix} = (U)(Z)_0^{-1}\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (K_4)\begin{pmatrix} I_{c1}^0 \\ I_{c2}^0 \end{pmatrix} = \underline{0} \tag{3-39}$$

may be grouped in a single matrix equation

$$\begin{pmatrix} (U)\left[(Z)_+^{-1} + (Z)_-^{-1} + (Z)_0^{-1}\right] & (K_1) & (K_3) \\ (U)(Z)_-^{-1} & (K_2) & 0 \\ (U)(Z)_0^{-1} & 0 & (K_4) \end{pmatrix}\begin{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \\ \begin{pmatrix} I_{c1}^- \\ I_{c2}^- \end{pmatrix} \\ \begin{pmatrix} I_{c1}^0 \\ I_{c2}^0 \end{pmatrix} \end{pmatrix} = \begin{pmatrix} -I_{s(0)} \\ -I_{r(0)} \\ 0 \\ 0 \\ 0 \end{pmatrix} \tag{3-40}$$

which can be solved for the required compensating currents.

It has been shown that permanent operation of a transmission line with only two phases, in a grounded system,

is possible by appropriate injection of compensating currents, $(I_{c1}^{-} + I_{c1}^{0})$ and $(I_{c2}^{-} + I_{c2}^{0})$ respectively, at its sending and receiving bus terminals.

Simplified Analysis

The tuning of the compensator to zero sequence currents, that is, its appearance as a short circuit to these currents, enables us to substitute the compensator by a short circuit in the zero sequence network. The modified equivalent network is now

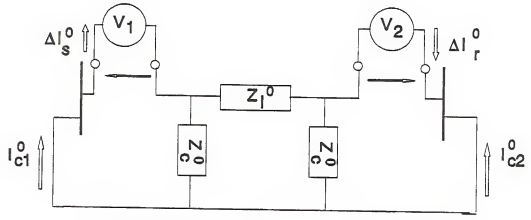

Fig.3-10. Reduced compensated zero sequence network under SPO.

The open pole condition still requires that

$$\begin{pmatrix} I_{as} \\ I_{ar} \end{pmatrix} = \begin{pmatrix} I_{s(0)} \\ I_{r(0)} \end{pmatrix} + \begin{pmatrix} \Delta I_s^{+} \\ \Delta I_r^{+} \end{pmatrix} + \begin{pmatrix} \Delta I_s^{-} \\ \Delta I_r^{-} \end{pmatrix} + \begin{pmatrix} \Delta I_s^{0} \\ \Delta I_r^{0} \end{pmatrix} = \underline{0} \qquad (3\text{-}41)$$

where as before

$$\begin{pmatrix}\Delta I_s^+\\ \Delta I_r^+\end{pmatrix} = (U)\,(Z)_+^{-1}\begin{pmatrix}V_1\\ V_2\end{pmatrix} \qquad \begin{pmatrix}\Delta I_s^-\\ \Delta I_r^-\end{pmatrix} = (U)\,(\bar{Z})_-^{-1}\begin{pmatrix}V_1\\ V_2\end{pmatrix}$$

(3-42)

and from Fig.3-10

$$\begin{pmatrix}I_{c1}^0\\ -I_{c2}^0\end{pmatrix} = \begin{pmatrix}\Delta I_s^0\\ \Delta I_r^0\end{pmatrix} = (\bar{Z})_0^{-1}\begin{pmatrix}V_1\\ V_2\end{pmatrix}$$

(3-43)

where $(Z)_0^{-1}$ is the two port impedance matrix of the zero sequence network as seen from the line terminals. Substituting (3-42) and (3-43) into (3-41) we obtain

$$\left[(U)\,(Z)_+^{-1} + (\bar{Z})_-^{-1} + (\bar{Z})_0^{-1}\right]\begin{pmatrix}V_1\\ V_2\end{pmatrix} = -\begin{pmatrix}I_{s(0)}\\ I_{r(0)}\end{pmatrix}$$

(3-44)

which can then be solved for the port voltages.

Positive Sequence Reactive Compensation

By virtue of the decoupling of the sequence networks, the expressions derived for the positive and negative sequence networks for the ungrounded system are also applicable here. Thus, (3-26) may be rewritten as

$$\begin{pmatrix}I_{c1}^+\\ I_{c2}^+\end{pmatrix} = (Y_1)_+\begin{pmatrix}V_1\\ V_2\end{pmatrix} + (Y_2)_+\begin{pmatrix}V_{s(0)}\\ V_{r(0)}\end{pmatrix}$$

(3-45)

substituting into (3-20)

$$\begin{pmatrix} \Delta I_{sT}^{+} \\ \Delta I_{rT}^{+} \end{pmatrix} = \left[(U)\,(Z)_{+}^{-1} + (K)_{+}(Y_1)_{+} \right] \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (K)_{+}(Y_2) \begin{pmatrix} V_{s(0)} \\ V_{r(0)} \end{pmatrix} \tag{3-46}$$

which when replaced, together with (3-33) and (3-36), into the expression for the phase currents at the open terminals, (3-41), yields

$$\left[(U)\,[(Z)_{+}^{-1} + (Z)_{-}^{-1} + (Z)_{0}^{-1}] + (K)_{+}(Y_1)_{+} \right] \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + (K_1)_{-} \begin{pmatrix} I_{c1}^{-} \\ I_{c2}^{-} \end{pmatrix} + (K_3)_{0} \begin{pmatrix} I_{c1}^{0} \\ I_{c2}^{0} \end{pmatrix}$$

$$= - \begin{pmatrix} I_{s(0)} \\ I_{r(0)} \end{pmatrix} - (K)_{+}(Y_2)_{+} \begin{pmatrix} V_{s(0)} \\ V_{r(0)} \end{pmatrix} \tag{3-47}$$

in conjunction with the requirements of no unbalanced currents flowing into the remote systems, (3-32), can be arranged in matrix form

$$\begin{pmatrix} \left[(U)\left[(Z)_{+}^{-1}+(Z)_{-}^{-1}+(Z)_{0}^{-1}\right]+(K)_{+}(Y_1)_{+} \right] & (K_1)_{-} & (K_3)_{0} \\ (U)\,(Z)_{-}^{-1} & (K_2)_{-} & 0 \\ (U)\,(Z)_{0}^{-1} & 0 & (K_4)_{0} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \\ I_{c1}^{-} \\ I_{c2}^{-} \\ I_{c1}^{0} \\ I_{c2}^{0} \end{pmatrix} = \begin{pmatrix} \begin{pmatrix} -I_{s(0)} \\ I_{r(0)} \end{pmatrix} - (K)_{+}(Y_2)_{+} \begin{pmatrix} V_{s(0)} \\ V_{r(0)} \end{pmatrix} \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \tag{3-48}$$

from which the unknown compensating currents may be found.

Steady State Results

A Fortran program has been written to compute the different compensator parameters and to evaluate their

sensitivity to various system conditions. Comparisons of the basic operational quantities are made between the uncompensated and the compensated network under the SPO condition. These variables include the phase voltage, real and reactive power, line phase and sequence currents and losses associated with the affected line.

The purpose of these comparisons is to demonstrate that, for a wide range of electric power system operating conditions and practices, selective sequence filtering is a viable concept. Selective sequence compensation provides the possibility of continuous power transfer when only two phases of a three phase circuit are available.

The base case corresponds to the grounded version of the equivalent system shown in Fig. 3-1. The receiving bus voltage is held at one per unit voltage and one per unit power at unity power factor is imported into the receiving terminal of the line. System parameters are as defined in Table 3-1 and during SPO the required compensator values are as indicated in Table 3-2.

Table 3-2. Reactive compensator values for the base case.

Buses	A-G (MVAR)	B-G (MVAR)	C-G (MVAR)	A-B (MVAR)	B-C (MVAR)	C-A (MVAR)
Sending	21.66	104.	-125.66	-526.33	83.66	442.33
Receiving	-28.33	-91.33	119.66	470.	1.33	-471.33

negative values = inductive VARS.

Positive sequence reactive compensation

By varying the amount of capacitance connected at the sending and receiving bus terminals of the line, under SPO conditions, it is possible to characterize its effect on the different system operating quantities. Increasing the shunt capacitance at the bus terminals of a line provides a way to increase the power transfer by raising bus terminal voltages. Fig.3-11 displays the percent negative and zero sequence current flow in the line, of pre-fault load current, under SPO condition and without selective sequence filtering, against positive sequence reactive compensation. The high percentage of negative sequence current flowing into the bus terminals generally exceeds that allowed by the continuous unbalance rating of a synchronous machine. Similarly, the zero sequence current flow generated by this condition may interfere with nearby communication circuits as well as ground protection schemes of nearby transmission lines.

Figures 3-12 and 3-13 show the variation in the MVAR requirement of the phase to ground and phase to phase compensating elements respectively, as the degree of shunt compensation (capacitive) is augmented. Per unit values indicated are on a single phase basis (1/3 of three phase MVA base), and corresponding to 333 MVAR. The compensator rating requirements at zero positive sequence capacitive reactance compensation (at the crossing of the vertical axis) correspond

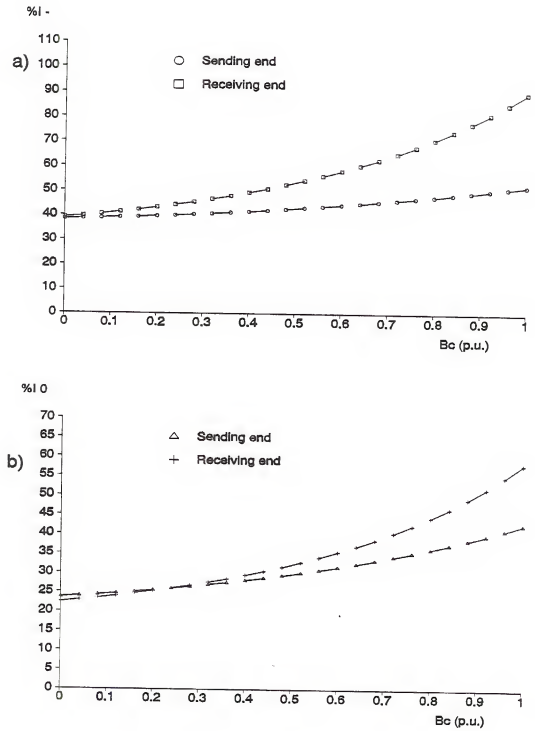

Fig.3-11. Percent sequence current at the sending and receiving bus terminals versus positive sequence reactive compensation, under SPO. a) negative sequence component and b) zero sequence component.

to those shown in Table 3-2 when expressed in per unit. It was previously demonstrated that in a line, under SPO with selective sequence compensation, the equivalent sending and receiving source impedances, in the negative and zero sequence networks, are in effect shorted out by the compensator. Thus, a balanced grounded three phase capacitor bank may be used to implement the reactive compensation in the positive sequence network.

The maximum percent change in voltage magnitude with respect to the pre-fault value, at the sending and receiving bus terminals, with and without selective sequence compensation, is depicted in Fig.3-14. The increase in voltage due to the shunt capacitor compensation is more pronounced in the uncompensated network because of its inherent unbalances.

A receiving to sending end source impedance ratio (Z_r/Z_s) of about 10/1 explains the larger variation in voltage at the receiving bus. More than a ten percent base of shunt capacitive compensation in the uncompensated network produces voltage changes over ten percent pre-fault, a figure normally exceeding the permissible operational limits. Notice that under selective sequence filtering, the amount of shunt compensation allowed before exceeding the ten percent mark is considerably greater than without filtering. These results demonstrate how positive sequence reactive compensation can be used to further increase power transfer, during SPO conditions, while maintaining tolerable voltage levels at the

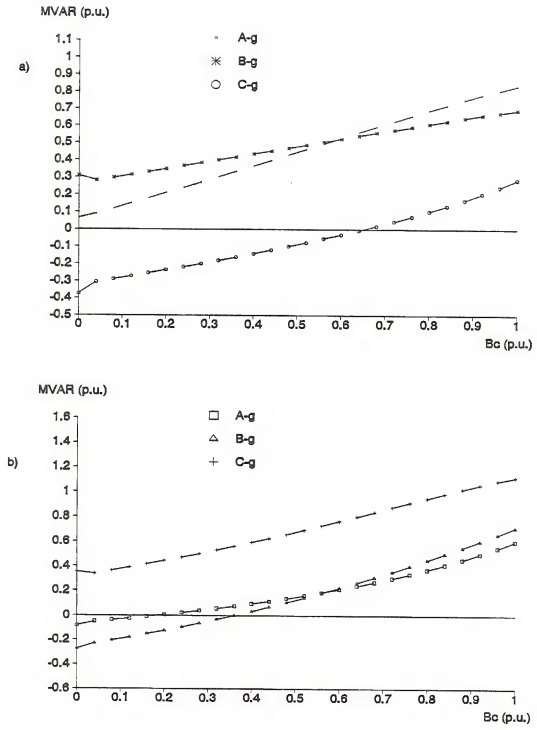

Fig.3-12. Phase to ground MVAR requirements of the selective sequence compensator under SPO at the a) sending and b) receiving end versus positive sequence capacitive reactance compensation. Base case data.

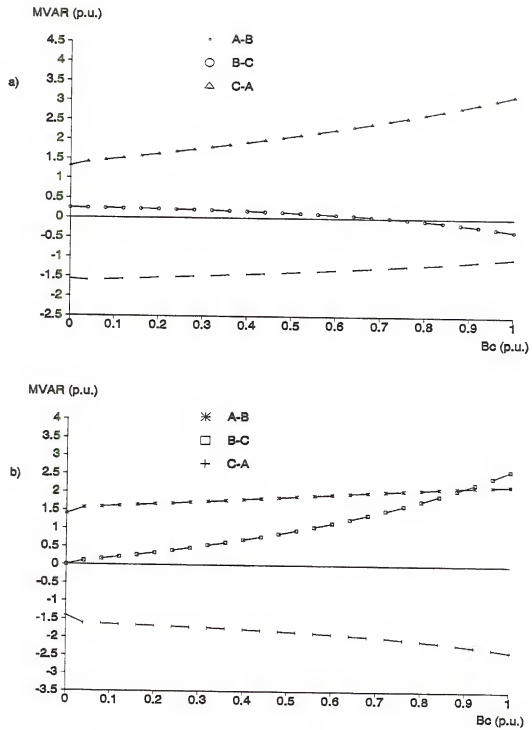

Fig.3-13. Phase to phase MVAR requirements of the selective sequence compensator under SPO at a) Sending and b) Receiving buses versus positive sequence reactive compensation. Base case data.

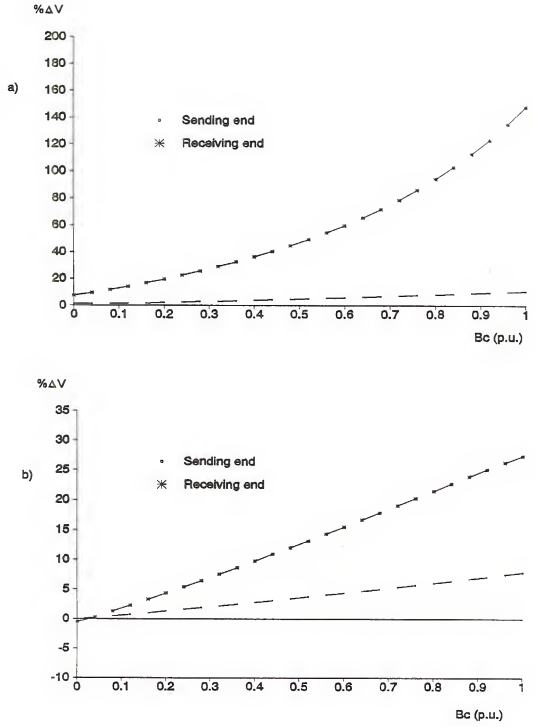

Fig.3-14. Maximum percent change in phase voltage at the sending and receiving terminals under SPO, a) without and b) with selective sequence current compensation versus percentage of positive sequence reactive compensation.

conditions, while maintaining tolerable voltage levels at the line terminals.

Figure 3-15 depicts the percent change in real power at the sending and receiving end terminals of the line, with and without selective sequence current filtering, versus shunt capacitance compensation. The reduction in real power variation, with respect to the pre-fault real power flow, is minimized as larger values of capacitance compensation are allowed. This is caused by the voltage boosting effect of the shunt capacitors. It is theoretically possible, as shown in Fig.3-15b, to maintain constant real power injection under SPO at either of the sending or receiving terminals. Higher line losses prevent this condition from ocurring simultaneously at both ends. Although an achievable state, maintaining constant real power injection at either of the line terminals may not be a desirable operating condition. The gain in power transfer capacity of the line under SPO may be offset by the increase in system losses associated with the reactive power injection. The optimum degree of shunt compensation will be that at which the incremental gain in real power transfer capacity of the line is equal to the incremental increase in system losses.

Percent change in line current and losses are shown in Fig.3-16 for the two conditions of interest. When selective filtering is used, it is seen that for the viable range of shunt compensation, that in which system voltages are between

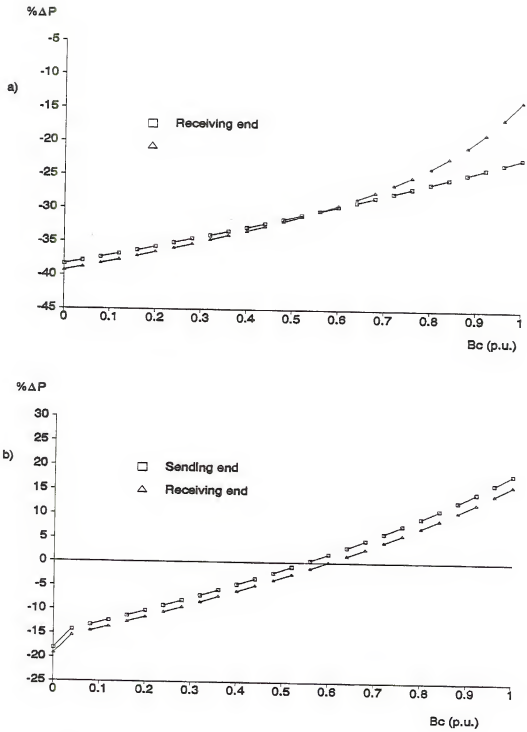

Fig.3-15. Percent change in sending and receiving real power during SPO a) without compensation and b) with sequence current compensation versus positive sequence reactive compensation.

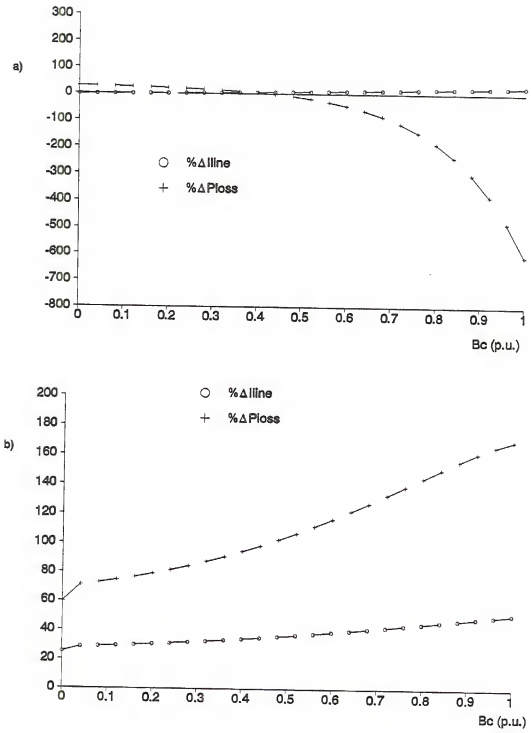

Fig.3-16. Maximum percent change in line current and percent change in line power losses during SPO a) without and b) with sequence current compensation versus positive sequence reactive compensation.

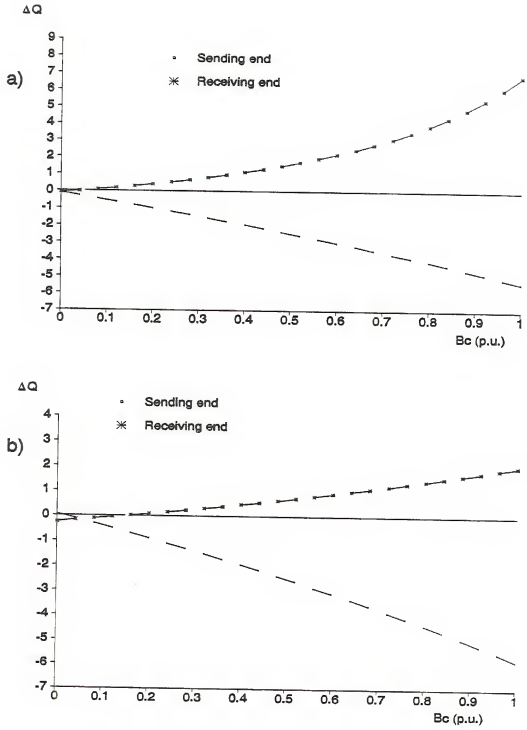

Fig.3-17. Change in reactive power at the sending and receiving ends of the line during SPO a) without and b) with sequence current compensation and versus positive sequence reactive compensation.

acceptable tolerances (~10%), the increase in line current and losses is within tolerable limits.

A plot of the change in reactive power flow, with respect to pre-fault value, into and out of the line terminals, under SPO and versus shunt capacitor compensation, is presented in Fig.3-17. As the vars generated by the shunt capacitors augment, more are forced to flow eventually into the line. In the following cases no positive sequence reactive compensation was used.

Line charging compensation

It is an accepted practice to partially compensate the charging capacitance of the line during light load conditions in order to maintain an adequate voltage profile. This is generally accomplished via a three phase grounded balanced reactor bank connected at each end of the line. The effect of such compensation, in our base case under SPO and selective sequence current filtering, is next analyzed.

The high percentage of negative and zero sequence current that flows into the sending and receiving end systems (Fig.3-18) precludes the operation of the line under SPO, irrespective of percentage of line capacitance compensation, without the use of selective sequence current filtering.

Figures 3-19 and 3-20 present, respectively, the required rating in MVAR of the phase to ground and phase to phase elements of the selective sequence compensators.

The compensator values at the vertical axis crossings correspond to those of Table 3-2. The relative insensitivity to the amount of line capacitance compensation used is particularly noticeable in the phase to phase units.

The maximum percent change in voltage magnitude with respect to the pre-fault value, at the sending and receiving bus terminals, with and without selective sequence compensation, is shown in Fig.3-21. It is seen that throughout the range of line capacitance compensation considered, the voltage variation is within acceptable limits when selective compensation is being used.

Figure 3-22 depicts the percent change real power, of pre-fault value, at the sending and receiving end terminals of the line, with and without selective sequence current filtering, versus line capacitance compensation. The reduction in power transfer remains essentially unaffected by the amount of line capacitance compensation used, when selective sequence filtering is not applied (Fig.3-22a). Percent real power change, when selective compensation is in use, stays relatively constant at about half the value of that which results when filtering is omitted.

When selective sequence filtering is in effect, during SPO, the percent change increase in line current and losses (Fig.3-23) remains within acceptable limits throughout the range of line capacitance compensation considered. Reduction

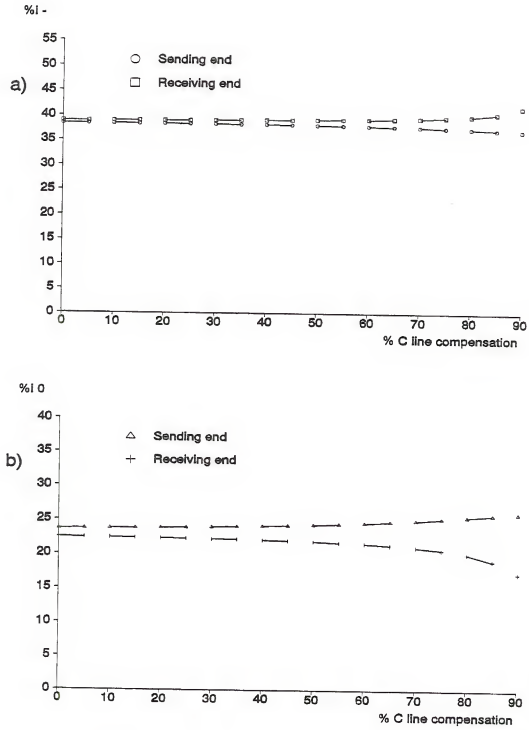

Fig.3-18. Percent sequence current at the sending and receiving bus terminals versus percentage of line capacitance compensated, under SPO. a) negative sequence component. b) zero sequence component.

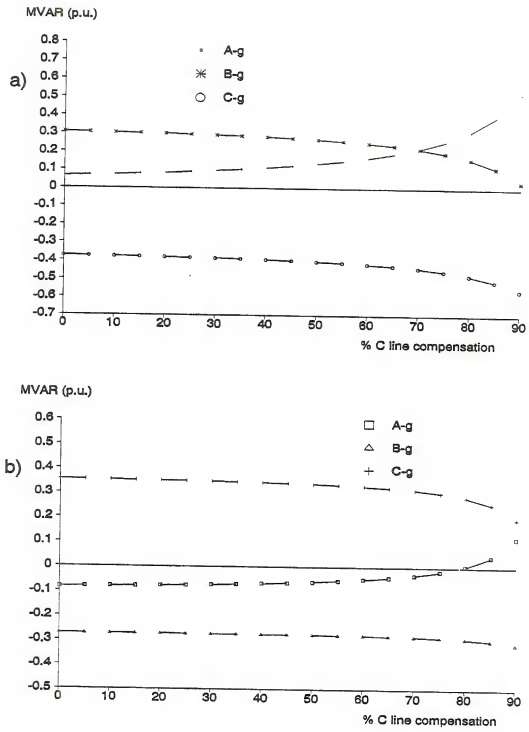

Fig.3-19. Phase to ground MVAR requirements of the selective sequence compensator under SPO, at a) the sending and b) receiving end, versus percentage of charging line capacitance compensated. Base case data.

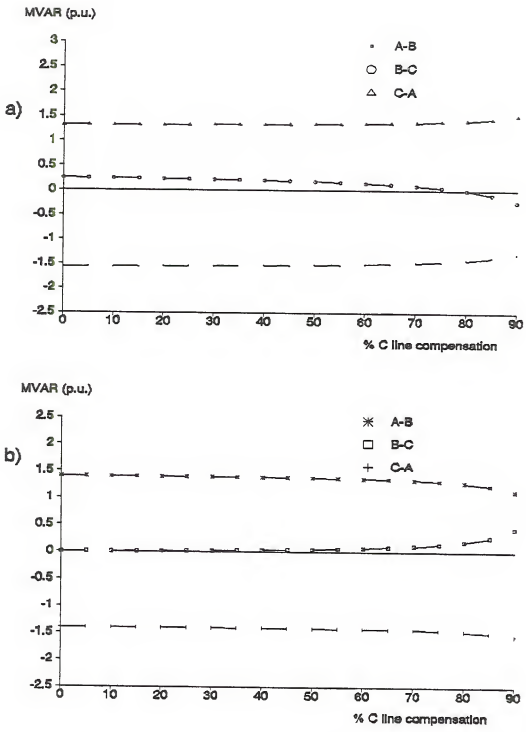

Fig.3-20. Phase to phase MVAR requirements of the selective sequence compensator under SPO at the, a) sending and b) receiving end, versus percent compensation of the line charging capacitance. Base case data.

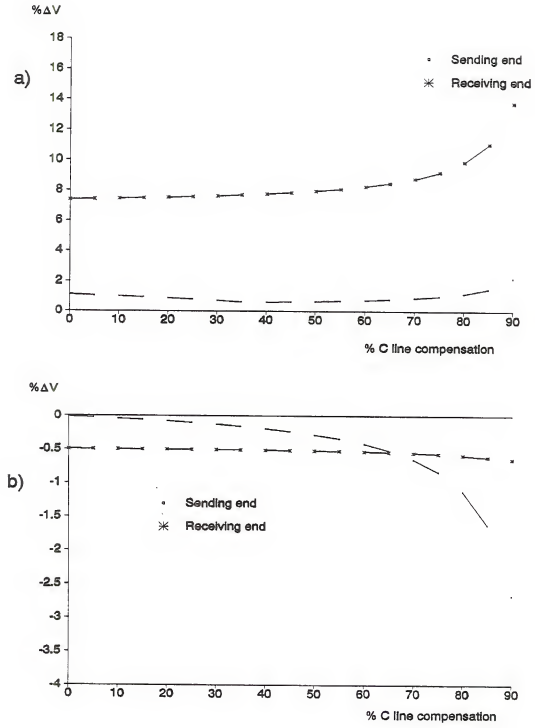

Fig.3-21. Maximum percent change in phase voltage at the sending and receiving terminals under SPO, a) without and b) with selective sequence compensation versus percentage of charging line capacitance compensated.

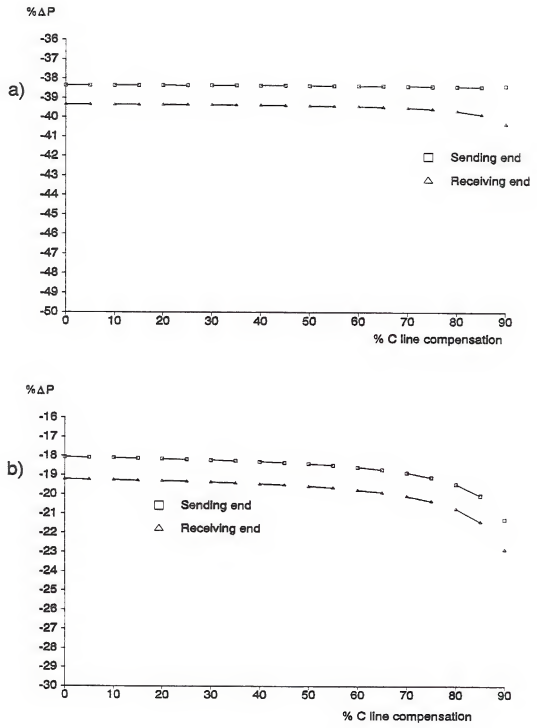

Fig.3-22. Percent change in sending and receiving real power during SPO a) without and b) with selective sequence compensation versus percentage of line capacitance compensated.

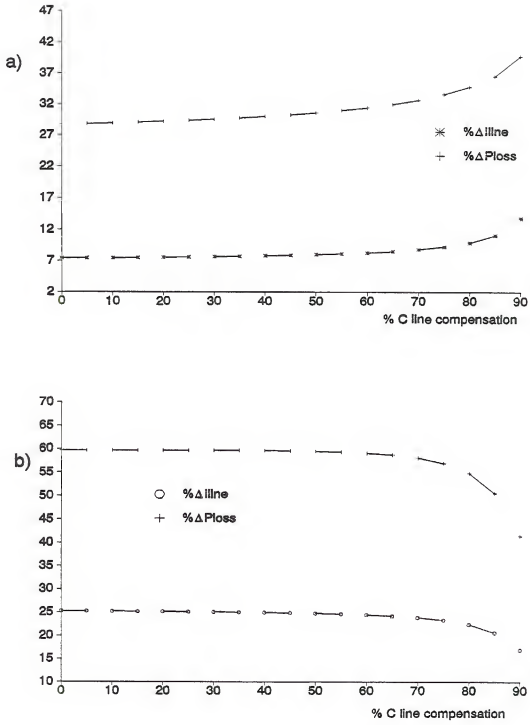

Fig.3-23. Maximum percent change in line current and line power losses during SPO a) without and b) with selective sequence compensation versus percentage of charging line capacitance compensated.

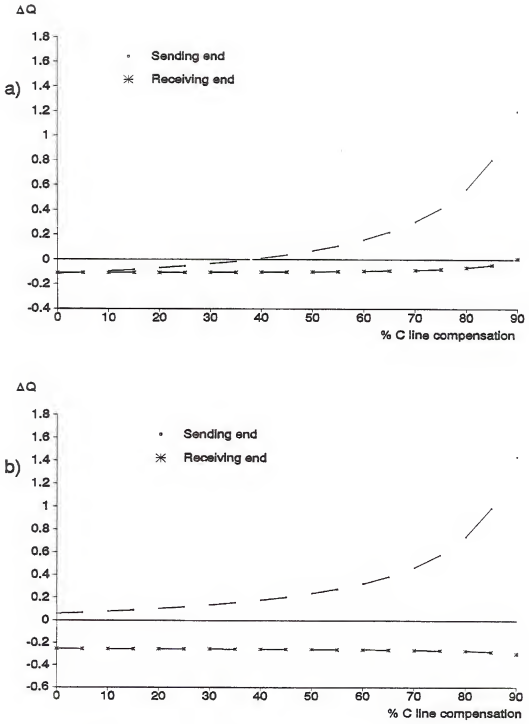

Fig.3-24. Change in reactive power at the sending and receiving ends of the line during SPO a)without and b) with sequence current compensation and versus percentage of line charging capacitance compensated.

in reactive power generated by the line is generally translated into a larger reactive power support requirement from the system. This trend is apparent in Fig.3-24. For the ranges of line capacitance compensation normally encountered (0-75%) the reactive power requirements from the system are within reasonable limits

Real power transfer

Real power transfer into the receiving terminal of the line was varied from 0.05 per unit to 1.0 per unit (@ unity power factor) in order to evaluate the effect of pre-fault load variation on the different system operating quantities, under SPO, and the selective sequence compensator MVAR requirements.

Graphs of the percentage negative and zero sequence currents, at the line terminals, during the SPO condition and as a function of the pre-fault real power flow (at unity power factor) are plotted in Fig.3-25. These are found to be relatively constant for the range of load currents considered. The phase to ground and phase to phase MVAR requirements for the selective sequence compensators are displayed in Fig.3-26 and 3-27, as a function of pre-fault real power flow into the the receiving bus. The MVAR requirements of the phase units associated with the open pole exhibit a linear increase with

load. The compensator values of Table 3-2 correspond to those shown at the one per unit load mark.

Figure 3-28 exhibits a graph of the maximum percent change in phase voltage magnitude with respect to the pre-fault value, at the sending and receiving bus terminals, with and without selective sequence compensation under SPO and against load variation at the receiving end. The voltage variation at both terminals, during SPO and for the full range of loads considered, is within the operational limits when the selective compensator is used.

Figure 3-29 depicts the percent change in real power at the sending and receiving end terminals of the line, with and without selective sequence current filtering, for different pre-fault load levels. By using selective sequence compensation, the deficit in power transfer is reduced to about one half of that obtained without filtering, for the load variations considered. Percent increase in line current and losses is again within reasonable levels as is shown in Fig.3-30.

The change in reactive power requirements at the sending and receiving bus during SPO and selective compensation is presented in Fig.3-31. The excess reactive power into the sending bus is gradually reduced as the load at the receiving terminal is augmented. MVAR support from the remote systems is inside acceptable limits.

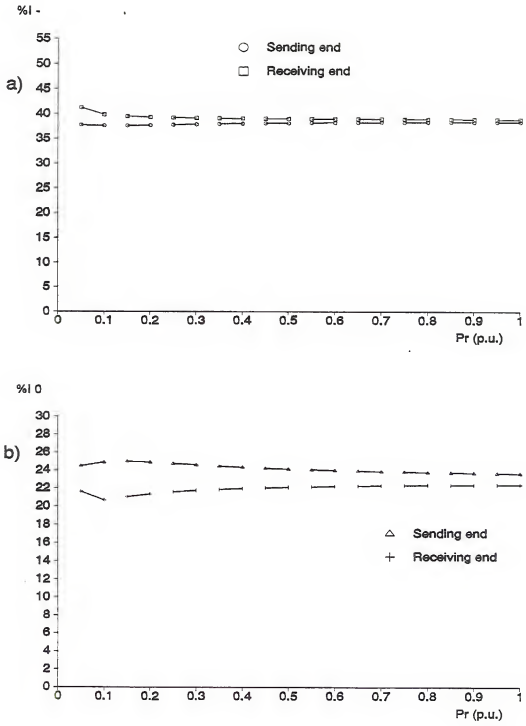

Fig.3-25. Percent sequence current at the sending and receiving bus terminals versus real power flow into receiving bus under SPO. a) negative sequence component. b) zero sequence component.

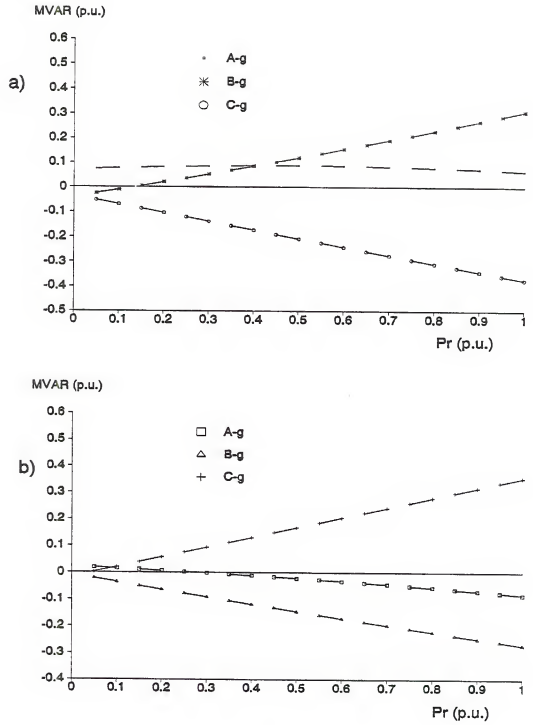

Fig.3-26. Phase to ground MVAR requirements of the selective sequence compensator under SPO, at the a) the sending and b) receiving end, versus real power flow into the receiving terminal.

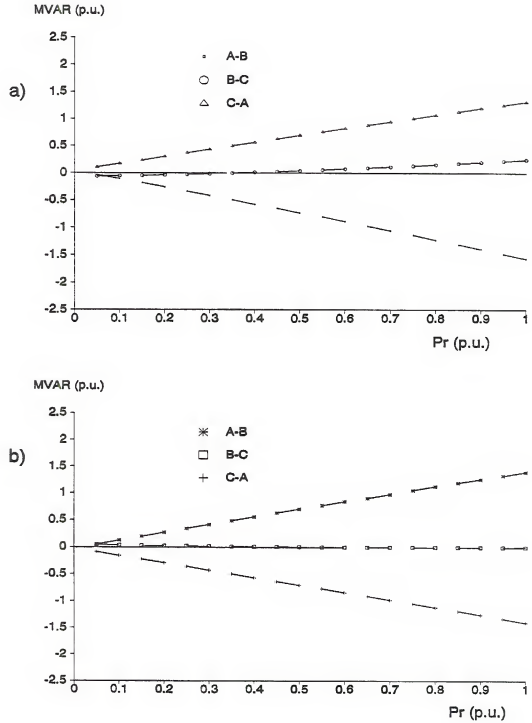

Fig.3-27. Phase to phase MVAR requirements of the selective sequence compensator under SPO, at a) the sending and b) receiving end, versus real power flow into the receiving terminal.

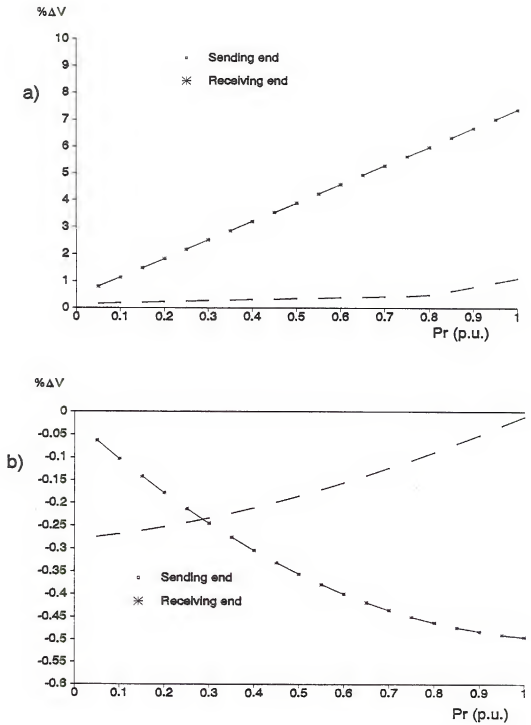

Fig.3-28. Maximum percent change in phase voltage at the sending and receiving terminals under SPO, a) without and b) with selective sequence compensation versus real power flow into the receiving bus.

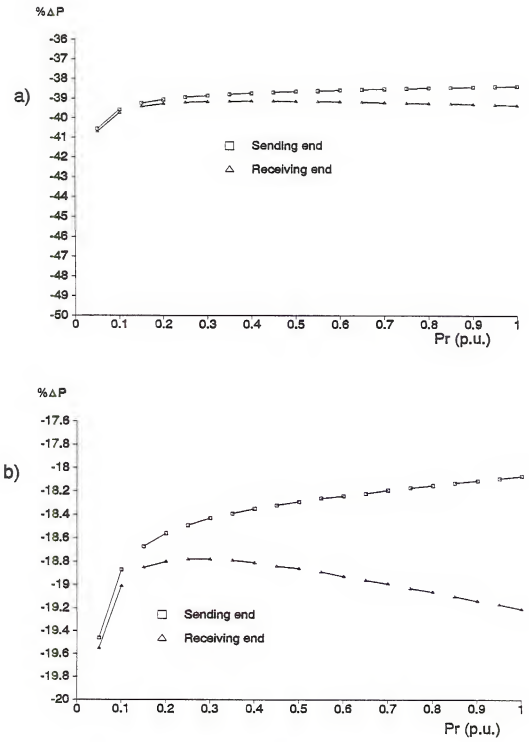

Fig.3-29. Percent change in sending and receiving real power during SPO a) without and b) with selective sequence compensation versus real power flow into the receiving bus.

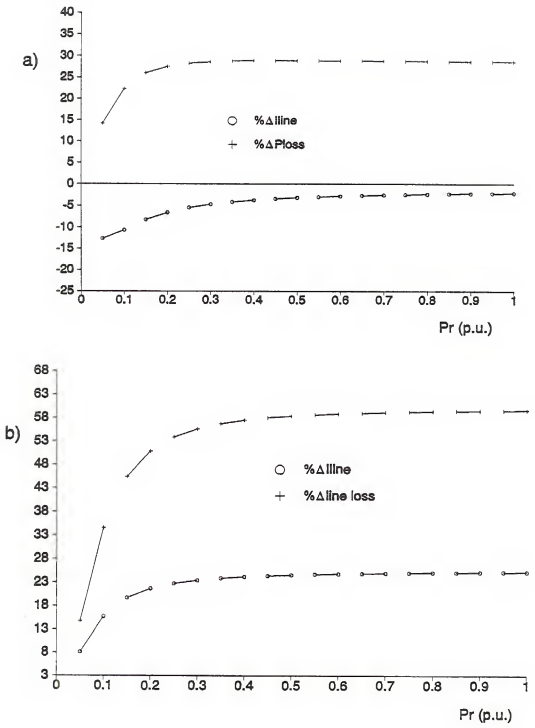

Fig.3-30. Maximum percent change in line current and line power losses during SPO a) without and b) with selective sequence compensation versus real power flow into the receiving bus.

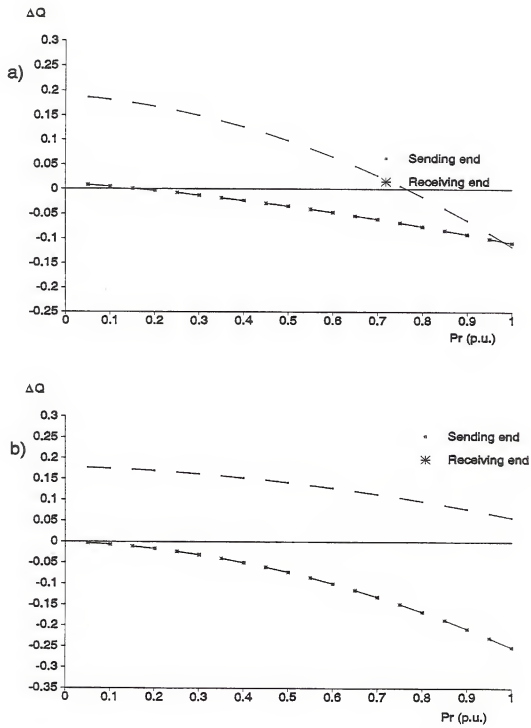

Fig.3-31. Change in reactive power at the sending and receiving ends of the line during SPO a) without and b) with sequence current compensation and versus real power flow into the receiving bus.

Series capacitance compensation

The effect of series compensation of the line reactance on our selective compensation scheme was studied next. Series capacitive compensation of the line reactance is an accepted practice in achieving higher power transfer capacities and better conductor utilization of high voltage transmission lines. By effectively shortening the electrical length of the line higher power transfer limits are obtained.

When selective sequence compensation is not in use, percent negative and zero sequence currents remain at undesirable levels as the degree of series compensation increases, as shown in Fig.3-32. The MVAR requirement for the phase to ground and phase to phase units of our selective sequence compensator stays relatively constant for the range of series compensation considered (Fig.3-33 and 3-34). The maximum percent change in phase voltage at either bus terminal, presented in Fig.3-35, remains within conventional boundaries.

Percent change in real power flow at the sending and receiving line terminals is reduced as the degree of series compensation is increased, with and without selective compensation. Reduction of the positive sequence reactance of the line, through series capacitor compensation, even under SPO and no selective sequence compensation provides a higher

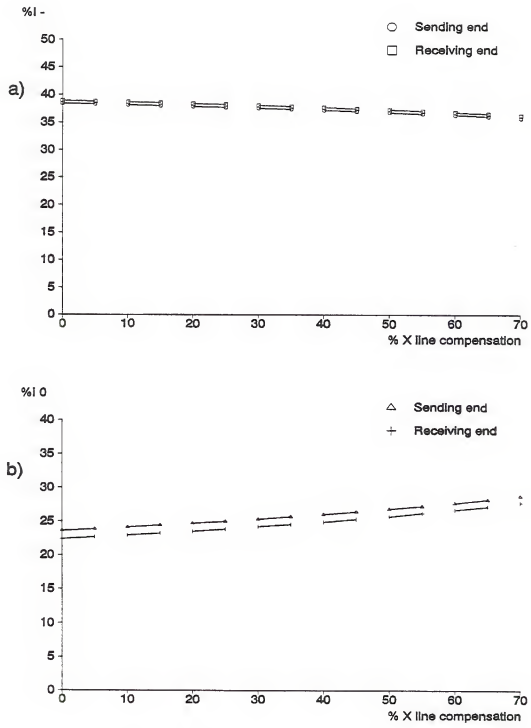

Fig.3-32. Percent sequence current at the sending and receiving bus terminals under SPO versus percentage of series compensation of the line. a) negative sequence component. b) zero sequence component.

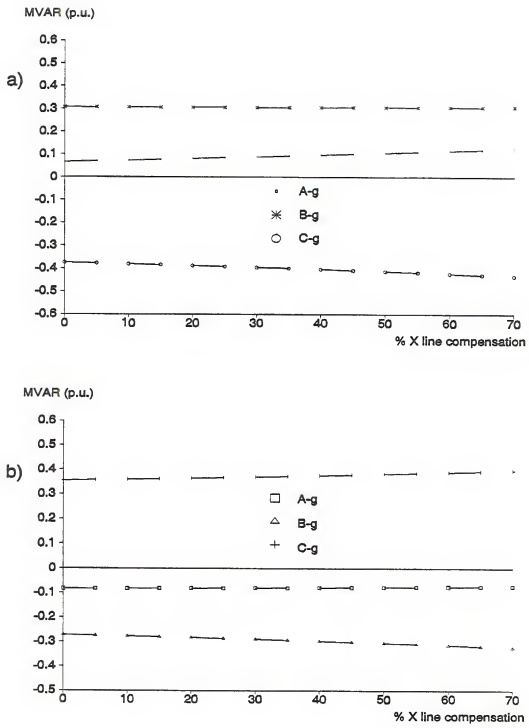

Fig.3-33. Phase to ground MVAR requirements of the selective sequence compensator under SPO at the a) sending and b) the receiving buses versus percentage of series compensation of the line.

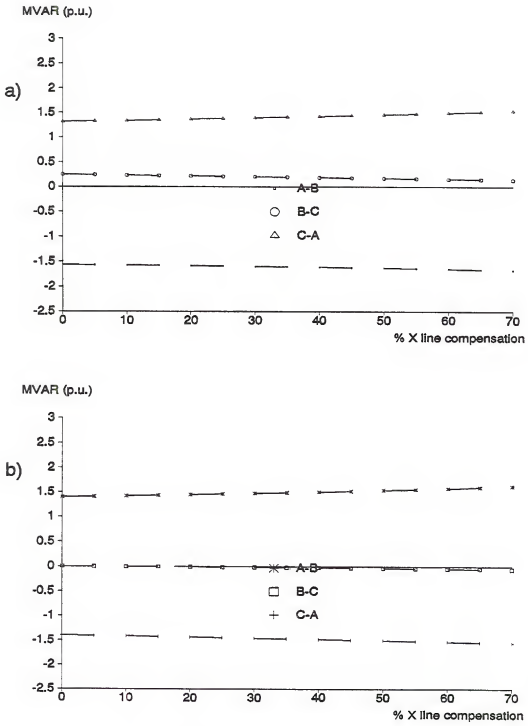

Fig.3-34. Phase to phase MVAR requirements of the selective sequence compensator under SPO at the a) sending and b) the receiving buses versus percentage of series compensation of the line.

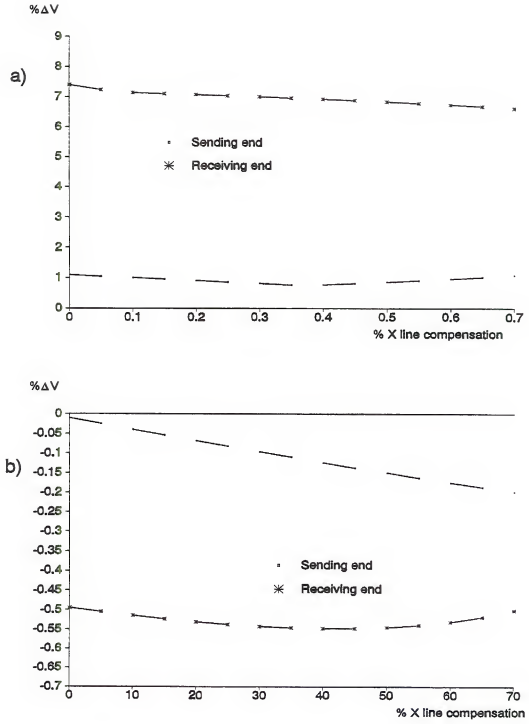

Fig.3-35. Maximum percent change in phase voltage at the sending and receiving terminals, under SPO, a) without and b) with selective sequence compensation versus percentage of series compensation of the line.

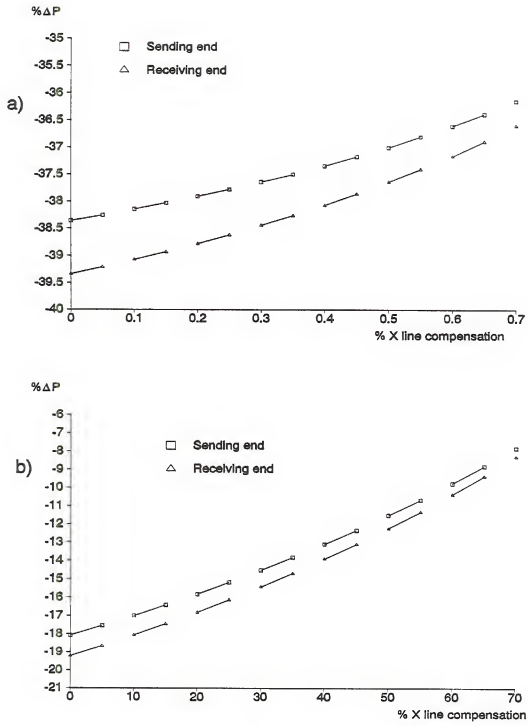

Fig.3-36. Percent change in sending and receiving real power during SPO a) without and b) with selective sequence compensation versus percentage of series compensation of the line.

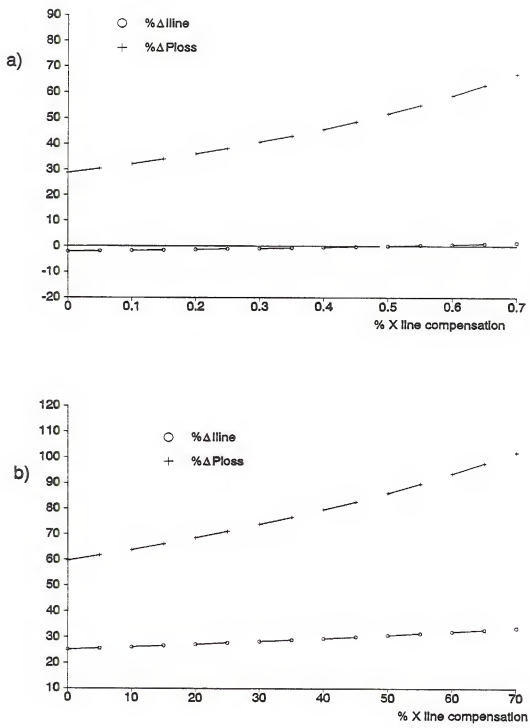

Fig.3-37. Maximum percent change in line current and line power losses during SPO a) without and b) with selective sequence compensation versus percentage of series compensation of the line.

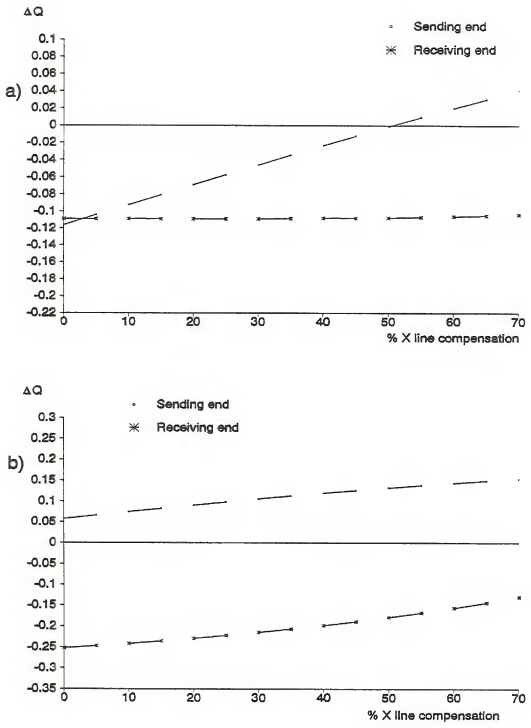

Fig.3-38. Change in reactive power at the sending and receiving ends of the line during SPO a) without and b) with sequence current compensation and versus percentage of series compensation of the line.

power transfer capacity as indicated in Fig.3-36. Recall that operation under SPO without selective sequence filtering will allow high percentages of negative and zero sequence currents to flow into the remote systems (Fig.3-32).

Percent variation in line current and losses during the SPO condition and selective sequence filtering is within tolerable limits for the range of series compensation studied, as Fig.3-37 indicates. Figure 3-38 displays the reactive power support requirements from the remote systems during SPO and selective compensation. These are within manageable limits for the size of the systems considered (short circuit capacity of 20 GVA and 2 GVA for the sending and receiving systems respectively).

Line length

Effects of varying the length of the line (10 -375 km.) are evaluated by considering a line with a configuration similar to that used in our base case (150 km.).

Pre-fault voltage and power transfer into the receiving bus is maintained at one per unit and unity power factor. The upper limit on the length of the line is based on a required line reactance, which when connected across rated line voltages having a 35° angle difference, determines a steady state power transfer of one per unit. The remaining parameters are as indicated for the base case.

Current unbalances in terms of the negative and zero sequence components, during SPO and no selective compensation, are included in Fig.3-39. The corresponding levels of unbalance are high enough to prevent permanent operation under SPO. Phase to ground and phase to phase MVAR requirements, for the selective sequence compensator at the sending and receiving buses, as a function of line length are displayed in Fig.3-40 and 3-41. The rating of the compensator tends to decrease with the length of the line. This suggests that the compensator might become a more attractive alternative for longer lines.

The percent change in phase voltage magnitude, at the sending and receiving terminals, remains within acceptable tolerances when selective compensation is in use for the range of line lengths studied (Fig.3-42). Power transfer is seen to decrease, in Fig.3-43, as longer lines are compensated. The series reactance of a line is proportional to its length. Longer lines have larger series reactances which, even under selective sequence compensation when operated under SPO, have a limiting effect in the power transfer capacity of the line. The relative sizes of the source impedances, as will be seen later, also dictates the change in the transfer capacity of the line under SPO. Percent change in line current and losses are shown in Fig.3-44 for the conditions of interest. Again, computed values are within practical operating limits.

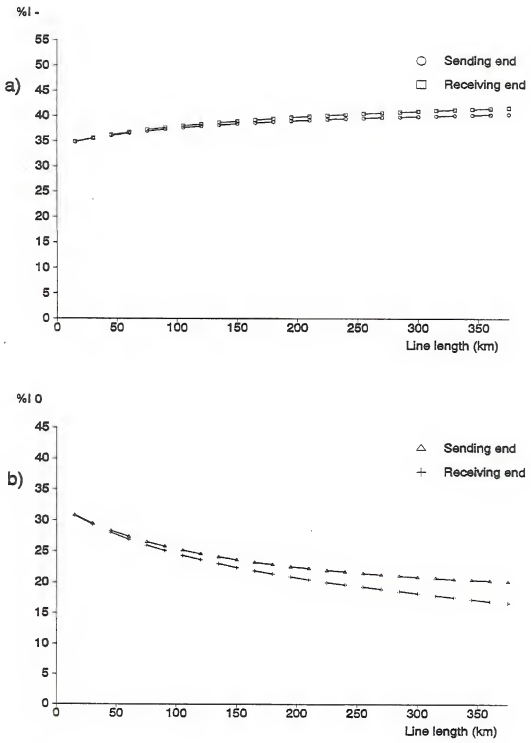

Fig.3-39. Percent sequence current at the sending and receiving bus terminals versus line length under SPO. a) negative sequence component. b) zero sequence component.

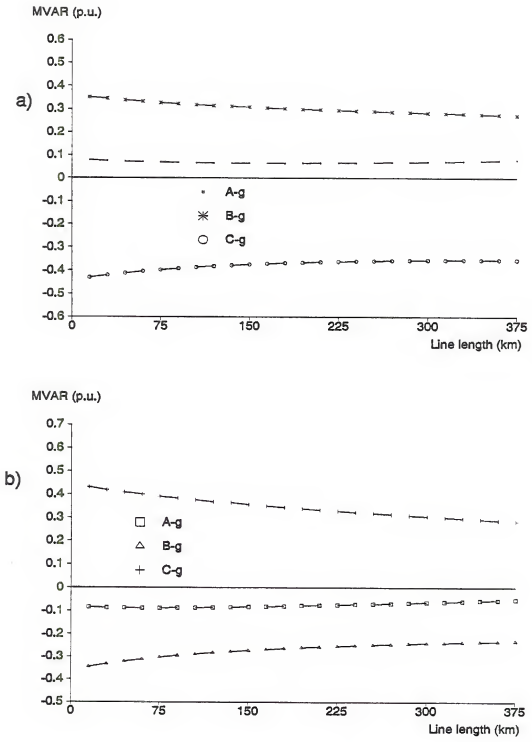

Fig.3-40. Phase to ground MVAR requirements of the selective sequence compensator under SPO at the a) sending and b) receiving buses versus length of line.

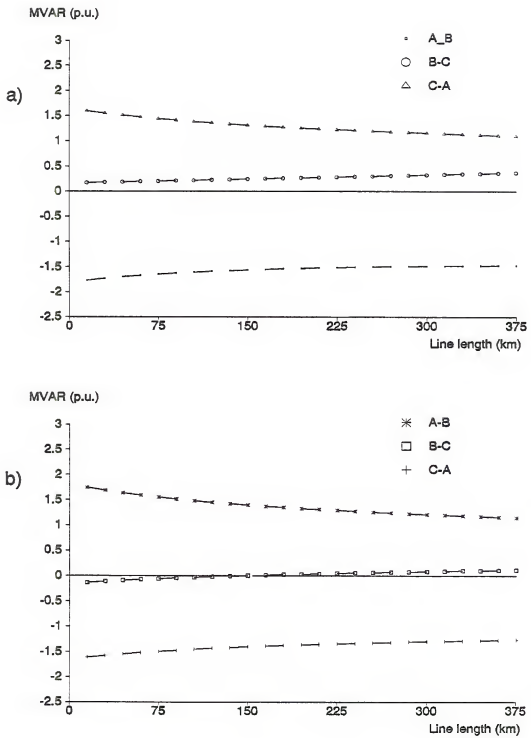

Fig.3-41. Phase to phase MVAR requirements of the selective sequence compensator under SPO at the a)sending and b)the receiving buses versus length of line.

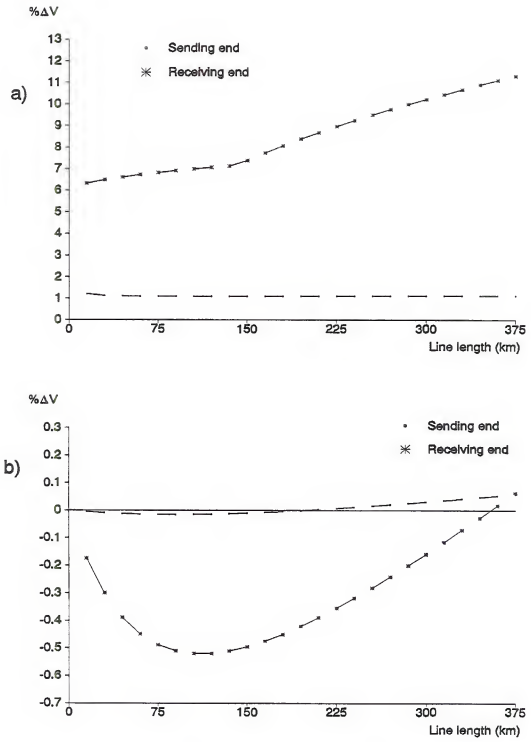

Fig.3-42. Maximum percent change in phase voltage at the sending and receiving terminals under SPO a) without and b) with selective sequence compensation versus length of line.

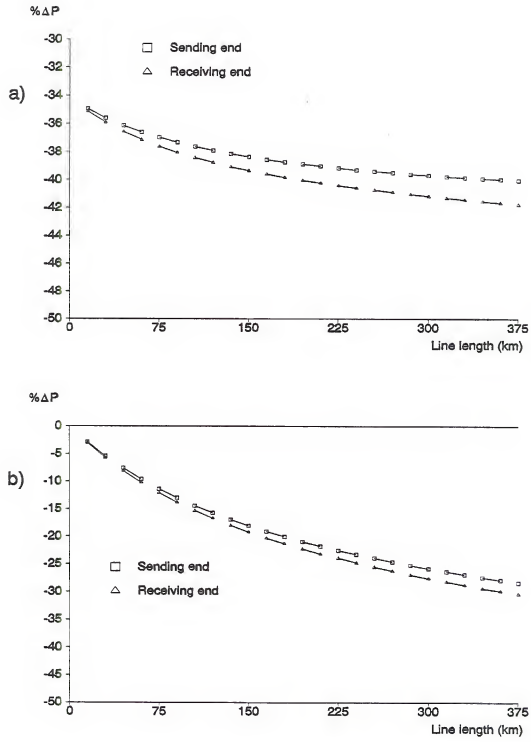

Fig.3-43. Percent change in sending and receiving real power during SPO a) without and b) with selective sequence compensation versus length of line.

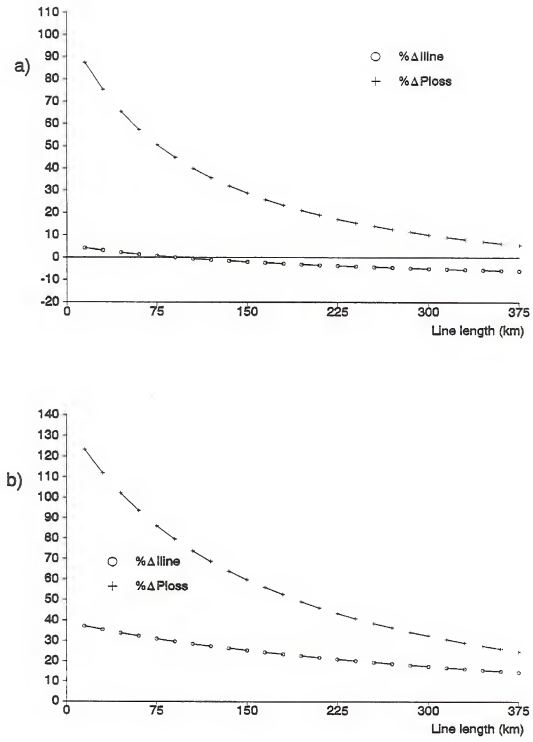

Fig.3-44. Maximum percent change in line current and losses during SPO a) without and b) with selective sequence compensation versus length of line.

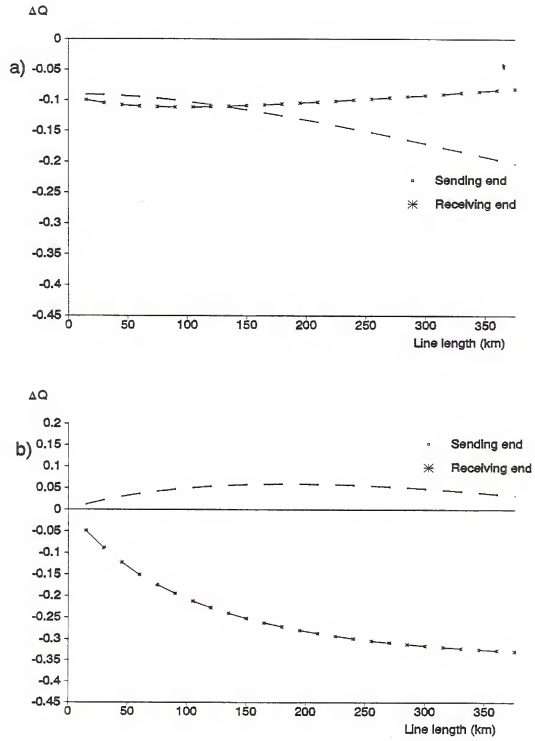

Fig.3-45. Change in reactive power at the sending and receiving ends of the line during SPO a) without and b) with sequence current compensation versus length of line.

Figure 3-45 presents a plot of the excess reactive power support required from the remote systems during SPO with and without sequence compensation. It is seen to be a small portion of the available short circuit duty at the bus terminals.

Source impedance ratio

For a fixed line impedance, the ratio of positive sequence receiving to sending source impedance is varied over a wide range of values in order to evaluate its effect in the system, under SPO, and in the selective sequence compensator proposed in this work. Two consecutive plots are given for each set of variables, one with the original sending end short circuit capacity (~20 GVA), and the second using a tenth of this value. The variation of the ratio of source impedances shown in the graphs safely cover the range of source impedances at these voltage levels for typical power systems. The lower limit in the source impedance ratio is indirectly determined by the available current interrupting capacity of the associated circuit breakers (about 60 GVA at this voltage level).

Voltage and real power transfer into the receiving bus is maintained at one per unit. Zero sequence source impedances are kept constant throughout this study since, in general, they are determined by grounding arrangements rather than source strength (generation capacity).

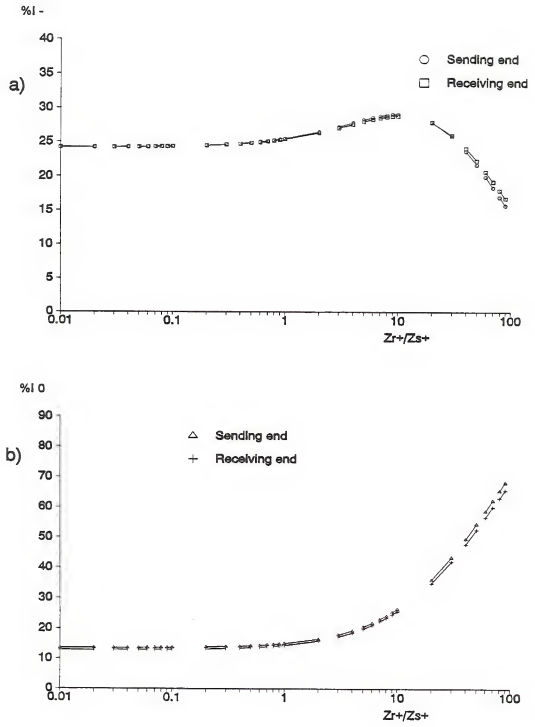

Fig.3-46. Percent sequence current at the sending and receiving bus terminals, under SPO, versus ratio of source impedances. a) Negative sequence component. b) Zero sequence component.

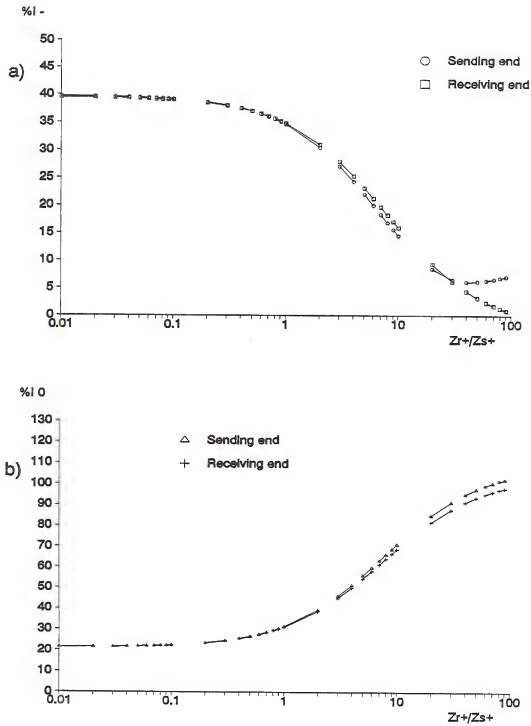

Fig.3-47. Percent sequence current at the sending and receiving bus terminals, under SPO, versus ratio of source impedances. a) Negative sequence component. b) Zero sequence component. (10 X Zs).

Percent negative and zero sequence currents, at the sending and receiving terminals of the line during SPO, versus the positive sequence source impedance ratio, for the indicated cases, are shown in Fig.3-47 and 3-48. As the relative size of the positive sequence impedance of the source at the receiving end increases the percentage of zero sequence current at the line terminals increases too. This is due to the shunting effect of the zero sequence network, which provides a lower impedance path to the flow of current than that of the negative sequence, in the network interconnection that represents the open pole condition.

MVAR requirements for the phase to ground and phase to phase elements of the compensator remain relatively constant for the two cases under consideration (Fig.3-48 through 3-51). There is a small increase in the rating of the compensator for large ratios of source impedances.

Percent change in phase voltage, during SPO and selective sequence compensation, stays within a one percent change as the ratio of source impedances is varied. This is true for both cases of positive sequence sending end source to line impedance considered (Fig.3-52 and 3-53). It is thus clear, that for a typical 500 KV line, selective sequence compensation, if applied during SPO conditions, will not produce unacceptable voltage variations in the system.

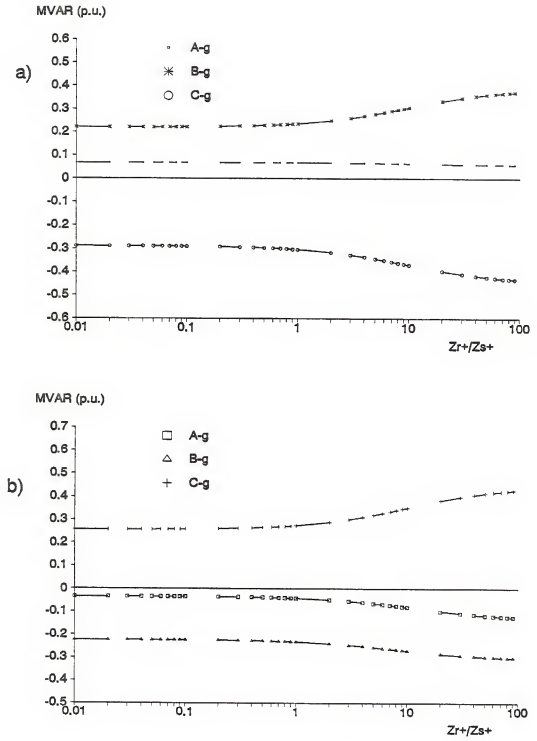

Fig.3-48. Phase to ground MVAR requirements of the selective sequence compensator under SPO at the a) sending and b) receiving buses versus ratio of source impedances.

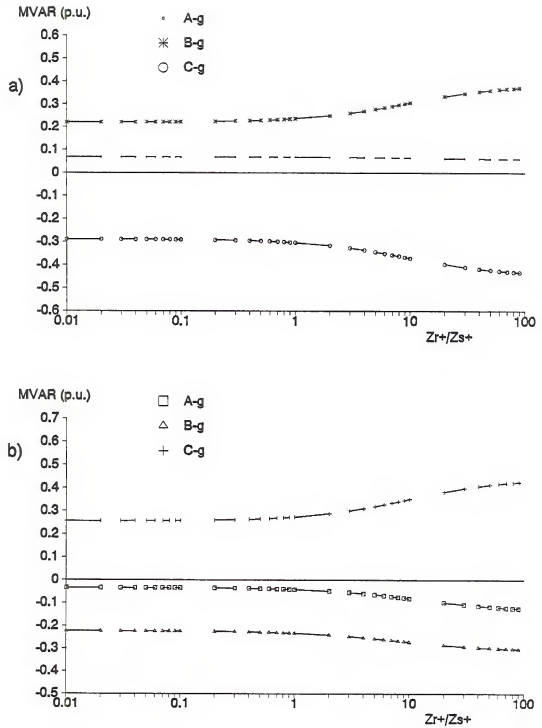

Fig.3-49. Phase to ground MVAR requirements of the selective sequence compensator under SPO at the a) sending and b) receiving buses versus ratio of source impedances. (10 X Zs).

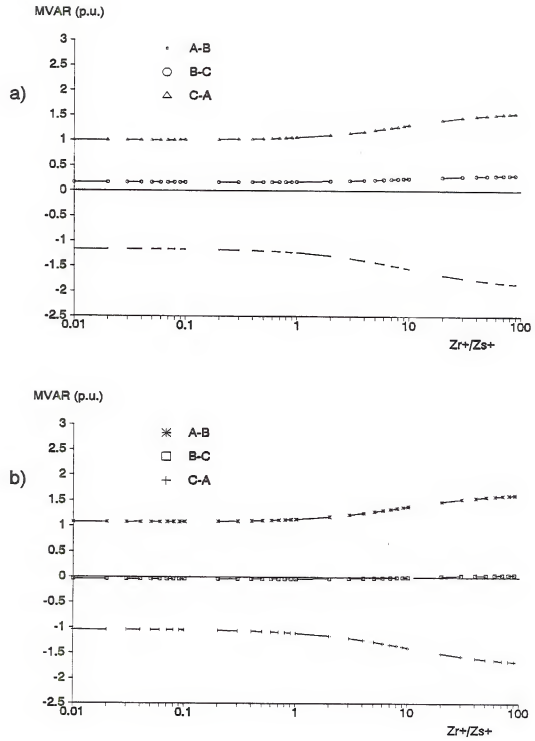

Fig.3-50. Phase to phase MVAR requirements of the selective sequence compensator under SPO at the a) sending and b) receiving buses versus ratio of source impedances.

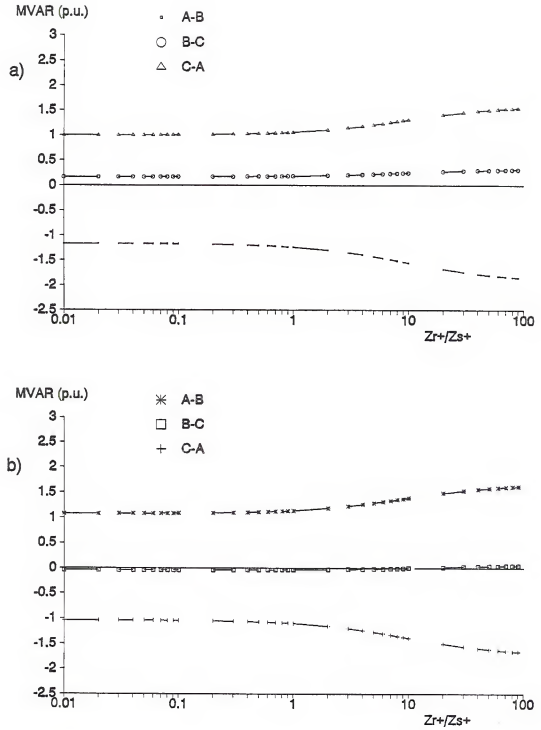

Fig.3-51. Phase to phase MVAR requirements of the selective sequence compensator under SPO at the a) sending and b) receiving buses versus ratio of source impedances. (10 X Zs).

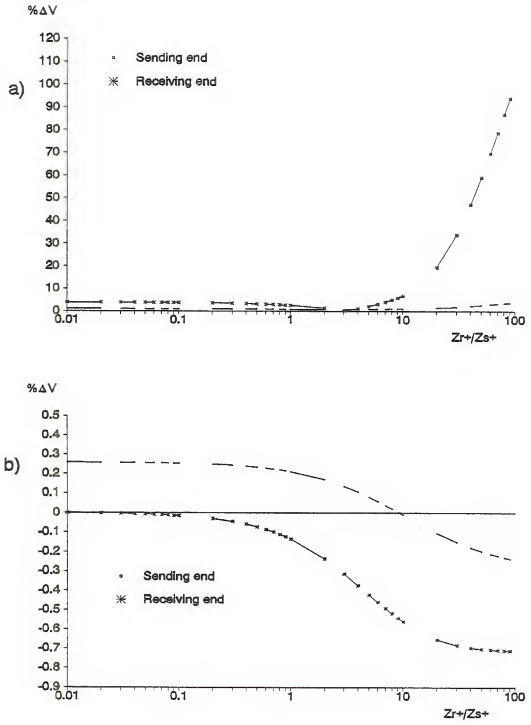

Fig.3-52. Maximum percent change in phase voltage at the sending and receiving terminals, under SPO a) without and b) with selective sequence compensation versus ratio of source impedances.

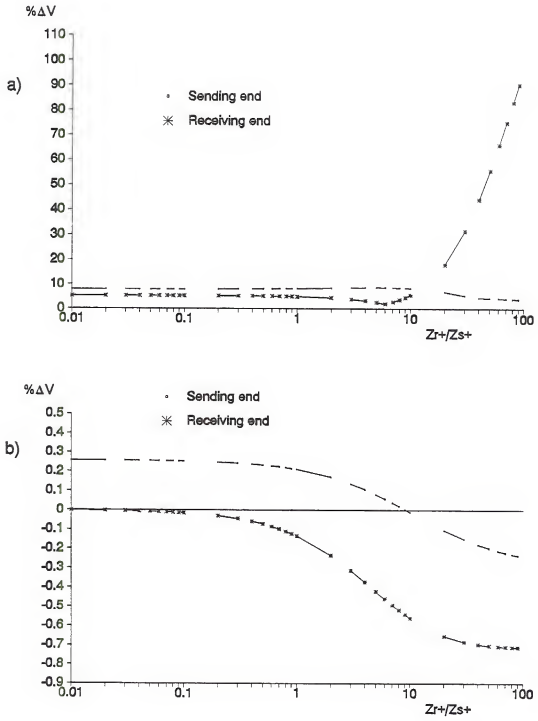

Fig.3-53. Maximum percent change in phase voltage at the sending and receiving terminals, under SPO a) without and b) with selective sequence compensation versus ratio of source impedances. (10 X Zs).

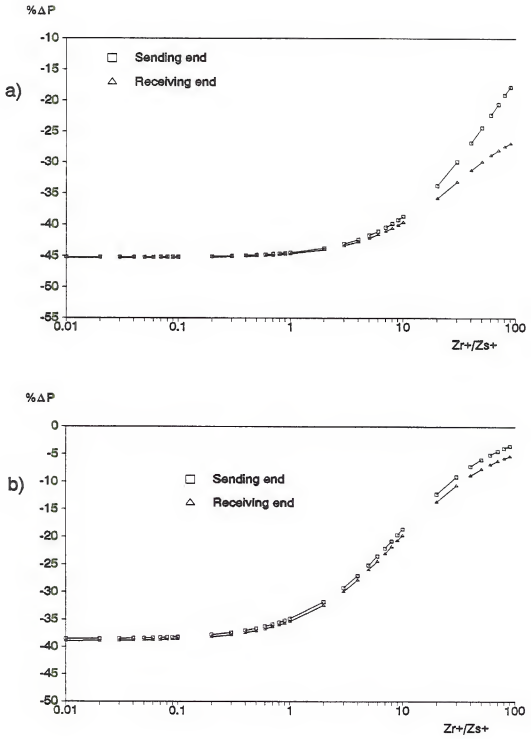

Fig.3-54. Percent change in sending and receiving real power during SPO a) without and b) with selective sequence compensation versus ratio of source impedances.

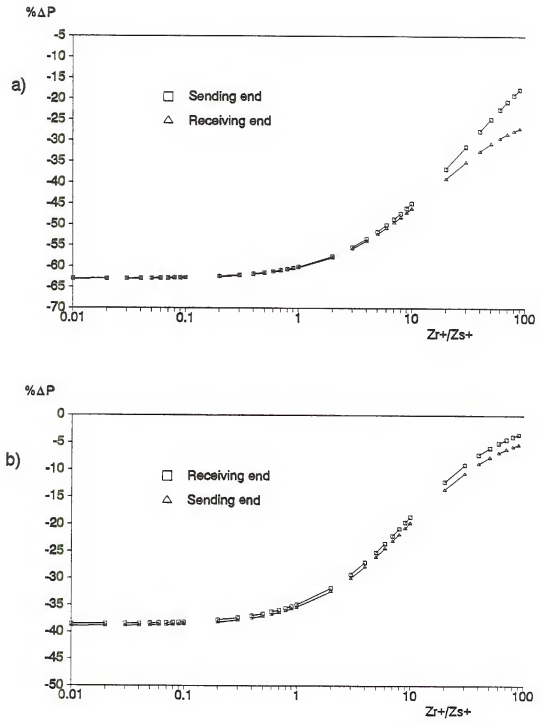

Fig.3-55. Percent change in sending and receiving real power during SPO a) without and b) with selective sequence compensation versus ratio of source impedances. (10 X Zs).

Figures 3-54 and 3-55 display the percent change in real power for the conditions already stated. Again the shunting effect of the zero sequence network provides a lower reduction in power transfer when large values of source impedances are in use. This is a result of the fact that changes in the positive sequence current, during SPO conditions are now severely limited by the source impedances. Note that even though a small reduction in power transfer is obtainable for large source impedance ratios when selective compensation is not used, the large variation in voltage (Fig.3-52a and 3-53a) precludes permanently operating the line under SPO.

Percent change in line current and losses are shown in Fig.3-56 and 3-57 for the conditions specified. Again, use of selective compensation results in tolerable values for the range of source impedance ratios utilized.

Figures 3-58 and 3-59 contain plots of the change in reactive power at the line terminals, during SPO with and without selective sequence compensation, for the specified conditions. It is seen that in order to maintain a small variation in the voltage at the line terminals during SPO and sequence compensation it becomes necessary to provide increasingly more reactive power support from the remote systems as the source impedance is increased.

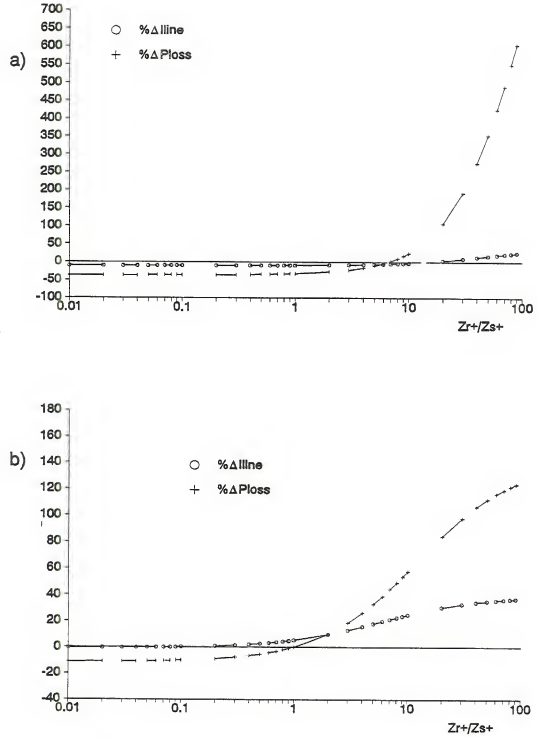

Fig.3-56. Maximum percent change in line current and losses during SPO a) without and b) with selective sequence compensation versus ratio of source impedances.

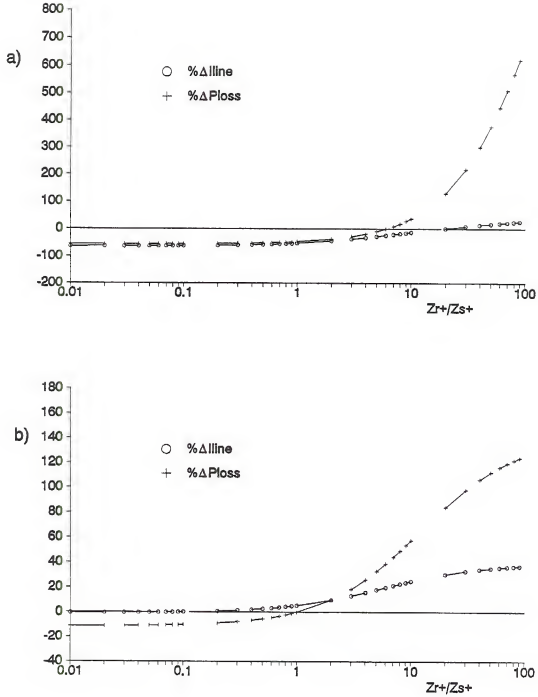

Fig.3-57. Maximum percent change in line current and losses during SPO a) without and b) with selective sequence compensation versus ratio of source impedances. (10 X Zs).

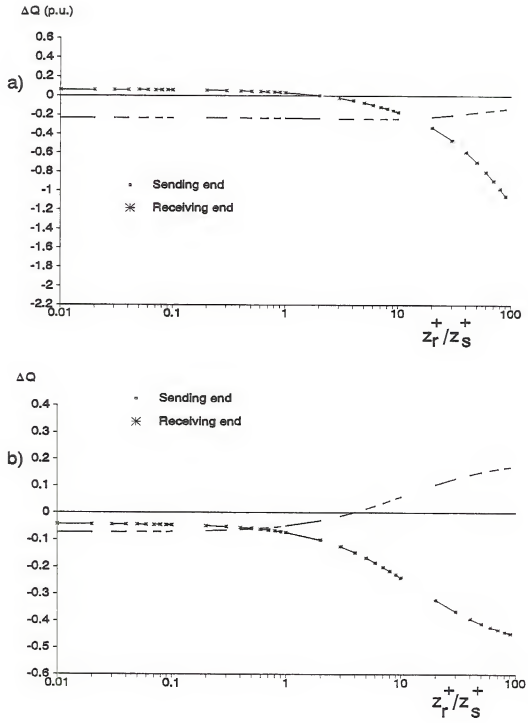

Fig.3-58. Change in reactive power at the sending and receiving ends of the line during SPO a) without and b) with sequence current compensation and versus ratio of source impedances.

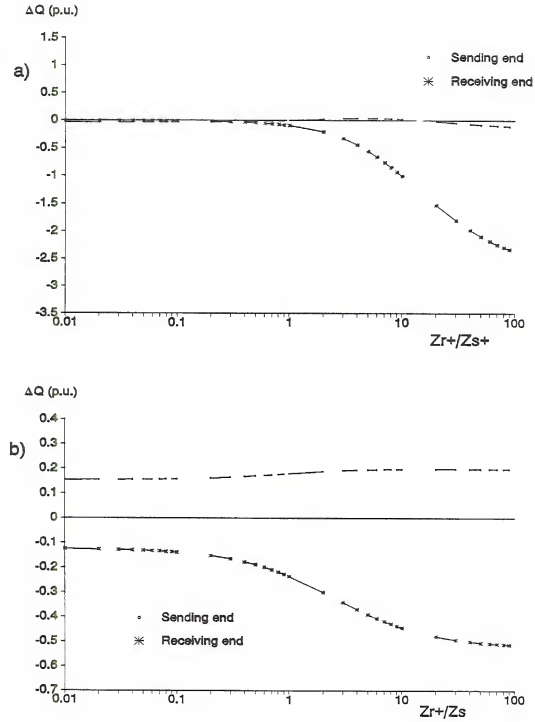

Fig.3-59. Change in reactive power at the sending and receiving ends of the line during SPO a) without and b) with sequence current compensation and versus ratio of source impedances. (10 X Zs).

CHAPTER 4
TIME SIMULATION

The Electromagnetics Transient Program (E.M.T.P) has been used to validate the results predicted by the proposed compensating scheme. By simulating the effects of selective sequence compensation in a transmission line used to interconnect either two infinite systems or a synchronous machine against an infinite system, we have corroborated the effectiveness of our approach to selective compensation for the most common equivalent system configurations. The composition of the compensator is computed in advance, for a prescribed initial condition of the system, for further use in the EMTP simulation runs. The selective sequence compensator used in these simulations is composed of fixed reactive elements that are simultaneously switched into the network at a pre-determined time, during the sequence of events associated with an SPO operation. No attempt is made to simulate a continuously adjustable or controllable impedance compensator that would selectively compensate under varying system parameters and operating conditions.

Initially, only ideal voltage sources are used to represent the remote equivalent systems in the simulation. This condition corresponds to generating sources being removed

far enough from the affected line so that variations in their impedances during system perturbations are absorbed by the impedances of the other components between them. The inertia of the corresponding systems is assumed large enough that the electrical frequency is forced to remain constant throughout the simulation period; the dynamics associated with the mechanical system are implicitly ignored.

A synchronous machine connected through a step up transformer and a transmission line to an infinite bus was also considered. An initial attempt is made to evaluate the electromechanical dynamics of this simple system to the various perturbations to which it is subjected during a typical compensation operation. The general system configuration studied corresponds to that shown in Fig.3-1, and the system parameter values unless otherwise stated to those presented in Table 3-1.

Interconnected Infinite Systems

Case Study # 1

Infinite inertial systems interconnected by a transmission line and with parameters corresponding to our base case configuration, as previously indicated, represented our first case of the time simulation runs. The initial conditions of the system correspond to a one per unit voltage at the receiving bus and a one per unit power (1000 MW) at

unity power factor being imported through the line into the receiving bus. The remaining voltages and currents of the equivalent system can be easily determined from these initial constraints. Table 4-1 contains the corresponding values for the initial conditions of the solved system.

In this first case, a solid phase A to ground fault is applied at the sending terminal of the line at t=25 msec after having achieved a pre-fault load level or steady state condition at t=0. The line protection is assumed to operate first at this terminal and opens the breaker pole associated with the faulted phase at t=48 msec. The receiving terminal follows, opening its associated pole at t=51 msec. The discrete selective compensator is switched in simultaneously at both bus terminals at t=100 msec. The compensator insertion resistor, used to provide damping to the high frequency transients originated during its energization and to prevent erroneous results from the simulation due to capacitor switching instabilities is switched out at t=250 msec. The time sequence of events is indicated in Fig.4-1.

Figure 4-2 and 4-3 present a plot of the instantaneous values of the phase voltages at the sending and receiving buses respectively. It is seen that the phase A voltage increases to about 2.5 per unit upon fault interruption. This condition is due to the lack of insertion resistors in the modeling of the opening pole sequence of the interrupter.

It should be mentioned that circuit breakers rated for operation at the 500 kV level are designed to withstand switching impulses of at least 2.6 per unit voltage crest between terminals with a pole open [10].

Table 4-1. Case Study I.
Initial conditions and post-fault steady state under SPO and selective sequence compensation.

		Line terminal voltage [kV]	Equivalent source voltage [kV]	Phase current source side of compensator [A]	Real Power at line terminals [MW]	Reactive Power at line terminals [MVAR]
Sending end	initial	509.5 @ 12.1 (1.019 p.u)	510.5 @ 14.6 (1.021 p.u)	1150.1 @ 9.8 (0.996 p.u)	1015 (1.015 p.u)	40 (0.04 p.u)
	post-fault	509.5 @ 12.5 (1.019 p.u)	510.5 @ 14.6 (1.021 p.u)	944.5 @ 8.5 (0.818 p.u)	831 (0.831 p.u)	59 (0.059 p.u)
Receiving end	initial	500 @ 0 (1.0 p.u)	543 @ -26.1 (1.086 p.u)	1154.7 @ 0 (1.0 p.u)	1000 (1.0 p.u)	0
	post-fault	497.5 @ -5.1 (0.995 p.u)	543 @ -26.1 (1.086 p.u)	942 @ 0.8 (0.816 p.u)	808 (0.808 p.u)	-84 (-0.084 p.u)

Furthermore, if surge arresters are applied for breaker protection, switching impulse restrictions disappear.

In a following case study, with breaker opening resistors included, the switching overvoltage is considerably reduced. Note that the relatively high transient voltage surge is due to the pole opening operation and not to the switching in of

the compensator. The voltages in all three phases at both sending and receiving terminals are seen to remain within acceptable limits when the compensator is connected. The rms values of the instantaneous phase voltages towards the end of the simulation coincide with those predicted by our steady state results. These are shown in Table 4-1.

Instantaneous values of the phase currents at the source side of the compensators, in the sending and receiving buses, are plotted in Fig.4-3 and 4-4. The current in phase A, drops to zero during the period from the last pole opening, at t=51 msec to that at which the selective compensator is switched in, t=100 msec. The observed offset in the current wave of some of the phases is due to the sudden energization of the inductive circuits of the sequence compensator.

The high frequency components present at this time, also coincide with the switching in of the compensator. These transients can be eliminated by synchronizing [11] the closure of the switch. Different closing schedules can be determined depending on the particular composition of the compensator. The optimum time for closure will depend on the nature of the Thevenin impedance as seen from the terminals of the pole being closed; if capacitive, closure should be attempted when the voltage across the pole is at a zero crossing, and if inductive if the voltage is at a peak.

A limit in the number of switch elements available in the EMTP version utilized, prevented a complete simulation run

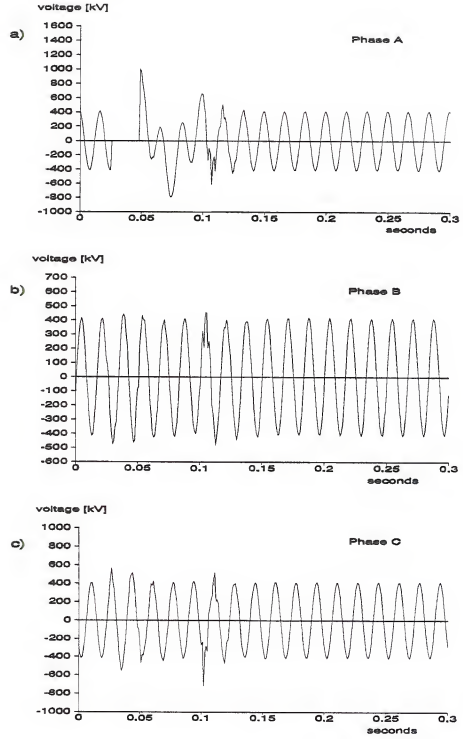

Fig.4-1. Instantaneous phase voltages at the sending terminal. a) Phase A, b) Phase B and c) Phase C.

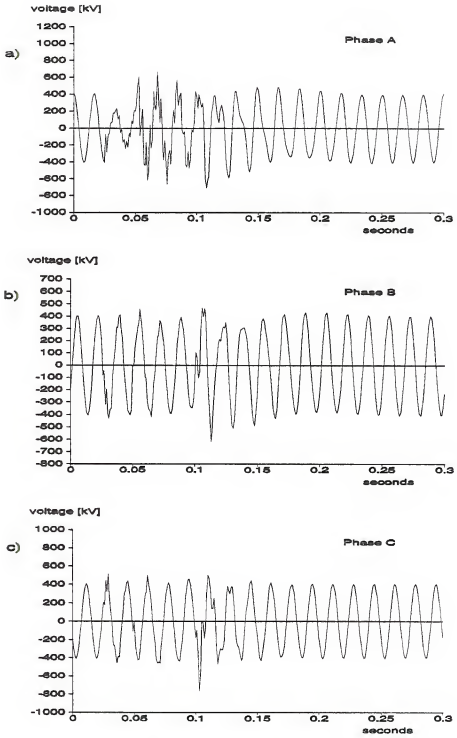

Fig.4-2. Instantaneous phase voltages at the receiving terminal. a) Phase A, b) Phase B and c) Phase C.

displaying the reduced transient and zero offset currents obtained by synchronous closing control of the selective compensator.

Figure 4-5 depicts the current that flows through the faulted terminal, from phase A to ground. In this case the fault was assumed to be permanent and solidly grounded in order to simplify the modeling, and to illustrate the electromagnetic intercoupling between the faulted phase and the remaining healthy phases.

The high frequency transients associated with capacitance switching at pole opening and under compensator energization are shown in Fig.4-5b. The steady state component of the current through the fault path, the secondary arc current that exists after pole opening and which results from the interphase capacitances and induction coupling with the unfaulted phases ,as previously mentioned, are also shown.

The instantaneous three phase power at the source side of the compensator, into and out of the line, is presented in Fig.4-6. The double frequency component associated with the unbalances generated by the fault and the single pole opening condition are clearly observed prior to the instant of selective compensation application. Average power transfer is considerably reduced during this period. High frequency transients are onset when the compensator is switched on and are gradually attenuated to the new steady state value of power transfer under SPO and selective compensation.

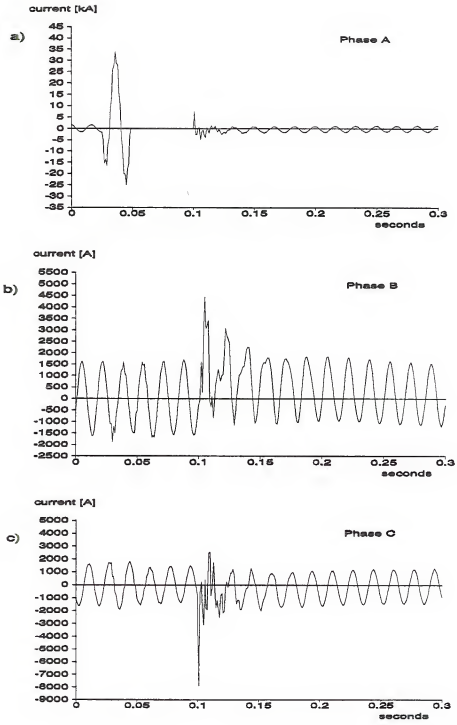

Fig.4-3. Instantaneous phase currents at the sending source side of the compensators. a) Phase A, b) Phase B, c) Phase C.

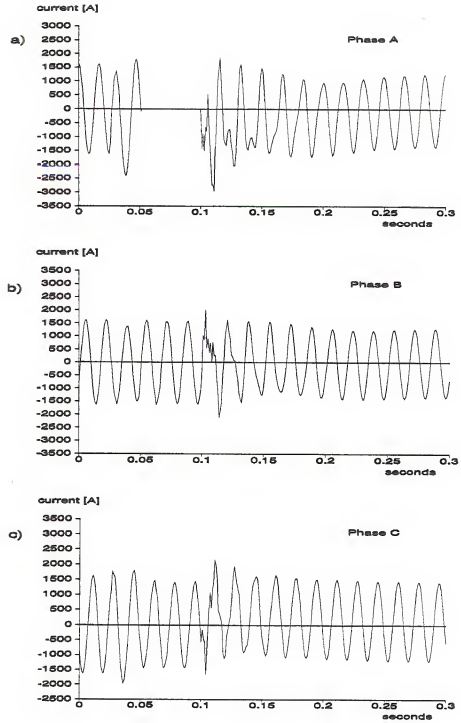

Fig.4-4. Instantaneous phase currents at the receiving source side of the compensator. a) Phase A, b) Phase B, and c) Phase C.

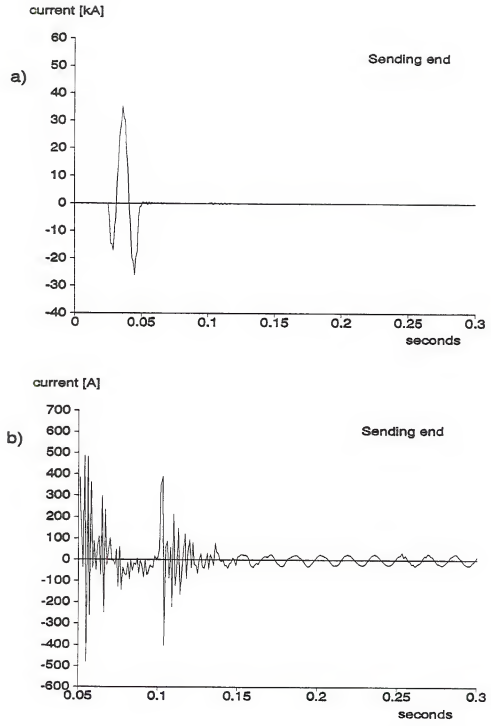

Fig.4-5. Instantaneous current at the fault terminals. a) Complete simulation period. b) Fault current values after SPO.

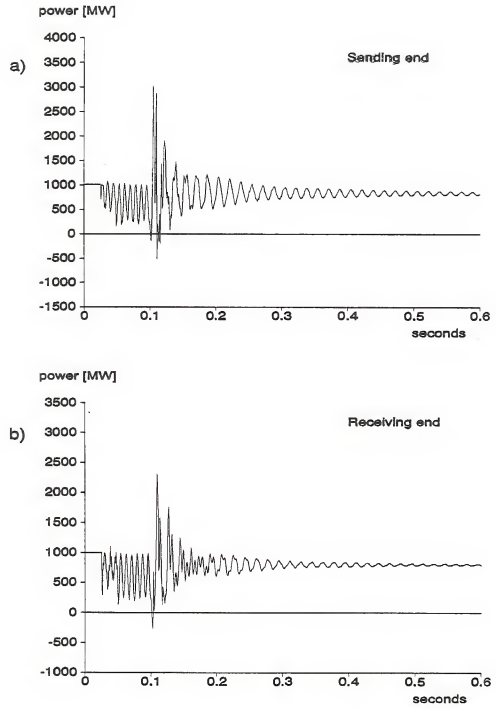

Fig.4-6. Instantaneous three phase power at the source side of the selective sequence compensator. a) Sending and b)
Receiving terminals.

A remarkable improvement in the quality and the magnitude of the power transfer through the line, after the switching transients have disappeared, is clearly apparent from the graph.

Case Study # 2

To illustrate some of the detrimental effects associated with operating a transmission line under SPO without selective compensation, a time simulation under these conditions of the system described in case study #1 was performed. Timing sequences and initial conditions remain as previously described with the exception of the compensator, which is not included in this case.

Figure 4-7a presents a plot of the instantaneous value of the negative sequence component of the current, at the sending terminals of the line, as a percentage of the pre-fault load current. The balanced pre-fault load conditions are implied in the zero magnitude of the negative sequence current content throughout this period. The high magnitude of the negative sequence current is associated with the flow of fault current, during the period before the associated breaker poles are opened. After fault clearing the remaining negative sequence current, at the line terminals, corresponds to the steady state value associated with operation of the line with an open pole. The instantaneous rms value of this signal is shown in Fig.4-7b. The final steady state value was seen to correspond

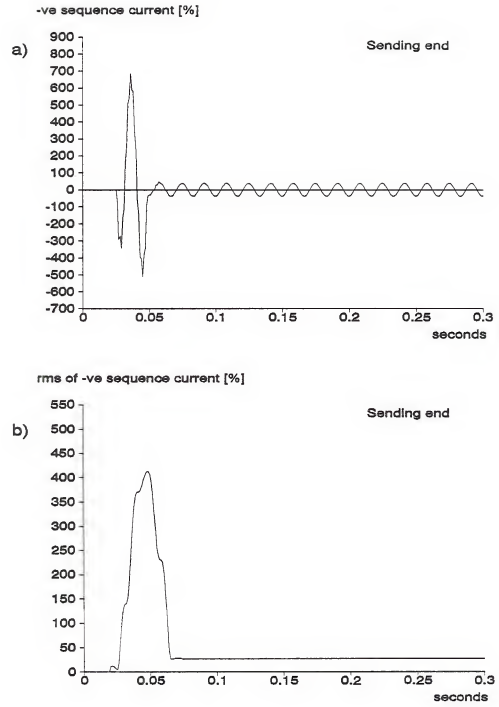

Fig.4-7. Instantaneous value of the negative sequence current at the sending terminal during SPO without compensation. a) Percent of pre-fault load current. b) Rms of percent value.

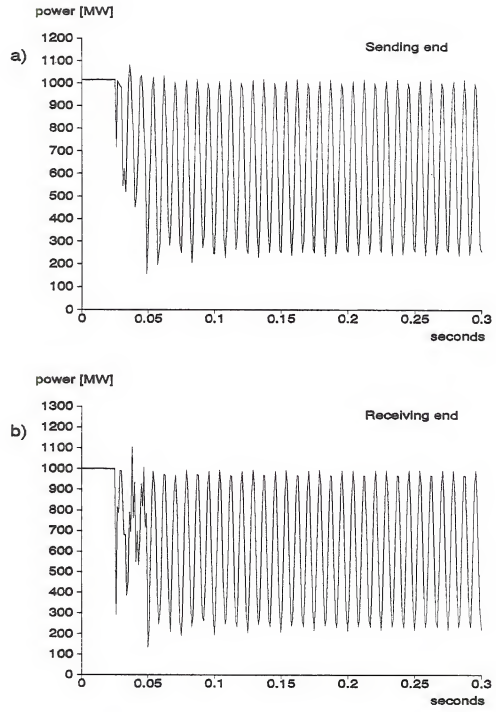

Fig.4-8. Instantaneous three phase power during SPO without selective sequence compensation. At the source side of the compensator in a) the sending and b) receiving end.

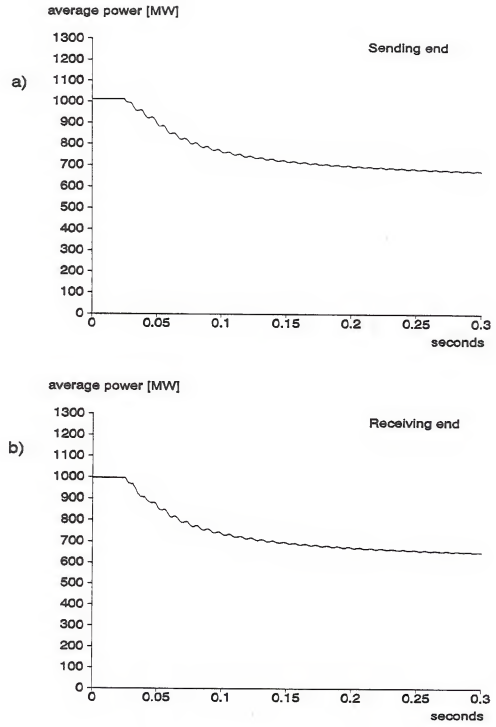

Fig.4-9. Instantaneous average power during SPO without selective sequence compensation, at the source side of the compensator in the a) sending and b) receiving terminals.

to that obtained through our steady state solution program and represented as the vertical axis crossing of the sending end %I. curve in Fig.3-11.

Figure 4-8 presents the instantaneous three phase power at the sending and receiving terminals of the line during the simulation period. The double frequency pulsating power, associated with the unbalanced conditions established once the fault has ocurred, is clearly observed in this graph. The corresponding average three phase power at both terminals is shown in Fig.4-9. The lower level of power transfer, reached during the unbalanced SPO operation, is evident at both terminals.

Case Study #3

The basic system configuration previously described is used once more. In order to simulate more realistic conditions, provisions have been taken to simulate the inclusion of series reactive compensation of the line, to provide a mechanism for secondary arc extinction and to incorporate breaker insertion resistors in the model. The steady state system operating values obtained during the pre-fault and post-fault stages of the simulation are shown in table 4-2. The post-fault values correspond to the line operated under SPO with selective sequence compensation.

By compensating the series inductive reactance of the line with series capacitors, the effective line reactance is reduced and, for a given phase angle difference between terminal voltages, the power transfer capacity of the line is augmented. For this case study, the line was assumed to be 70% series compensated.

High voltage transmission lines equipped with single pole autoreclosure facilities, unless of short length or of low rated voltage, will normally require having some means for extinguishing the follow up or secondary arc current flowing through the arc path of the fault current after the associated poles at the line terminals have opened. High speed grounding switches (H.S.G.S) [4] constitute an effective means to extinguish the secondary arc current. By forcing the recovery voltage across the secondary arc path to remain at a low value, the secondary arc current is reduced to self extinghishing levels. To simulate the application of our selective compensator under a more realistic scenario, H.S.G.S was adopted as the method to guarantee secondary current extinction.

To diminish the switching overvoltages, generated when the affected poles are opened to clear the fault, breaker pre-insertion resistors have also been modeled for this case. The use of pre-insertion resistors [12,13] is an established method for reducing transient overvoltages developed during

breaker switching operations. By appropriate sizing of these elements, the undesirable effects of current re-strikes and re-ignitions during pole opening and closing can be avoided.

The time sequence of events pertaining to this simulation is as follows:

t = 25 msec. A solid phase A to ground fault is applied at the sending terminal of the line.

t = 48.7 msec. The phase A pole opening resistor is inserted at the sending end.

t = 50.8 msec. The phase A pole opening resistor is inserted at the receiving end.

t = 54.1 msec. Phase A pole opening, at the sending end, is completed.

t = 65.4 msec. Phase A pole opening, at the receiving end, is completed.

t = 70 msec. Phase A high speed grounding switch at the receiving end is closed.

t = 100 msec. Selective sequence compensator is switched in at both sending and receiving buses.

t = 250 msec. Insertion resistors of the compensator are bypassed.

Without loss of generality the switch that simulates the fault inception is also used to represent the high speed grounding switch at the sending end. A limit in the dimensioning of the available EMTP version prevented the use of a separate unit.

Table 4-2. Case Study III.
Initial conditions and post-fault steady state
under SPO and selective sequence compensation.
Series compensation and H.S.G.S.

		Line terminal voltage [kV]	Equivalent source voltage [kV]	Phase current source side of compensator [A]	Real Power at line terminals [MW]	Reactive Power at line terminals [MVAR]
Sending end	initial	500.5 @ 3.66 (1.001 p.u)	498.5 @ 6.3 (0.997 p.u)	1165.1 @ 9.7 (1.009 p.u)	1004 (1.004 p.u)	-110 (-0.11 p.u)
	post-fault	499.5 @ 3.87 (0.999 p.u)	498.5 @ 6.3 (0.997 p.u)	1072.7 @ 7.3 (0.929 p.u)	926 (0.926 p.u)	-56 (-0.056 p.u)
Receiving end	initial	500 @ 0 (1.0 p.u)	543 @ -26.1 (1.086 p.u)	1154.7 @ 0 (1.0 p.u)	1000 (1.0 p.u)	0
	post-fault	497.5 @ -2.3 (0.995 p.u)	543 @ -26.1 (1.086 p.u)	1065 @ 0.6 (0.923 p.u)	917 (0.917 p.u)	-43 (-0.043 p.u)

Figures 4-10 and 4-11 show the instantaneous phase voltages at the sending and receiving buses for the present case. It is seen that the use of a pole opening resistor has practically eliminated any switching overvoltage during fault clearing. Switching overvoltages at compensator insertion are within the withstand capability of the interrupter. The steady state voltage towards the end of the simulation is inside system operating constraints.

Instantaneous values of the phase currents at the source side of the compensator in the sending and receiving ends are plotted in Fig.4-12 and 4-13 respectively. The pre-fault and fault currents as well as the zero current interval of the faulted phase, the time period between fault clearing and compensator reconnection, are clearly depicted in Fig.4-12a.

The high frequency transient currents generated during compensator insertion are due to the energizing of the capacitive reactance of the filter at other than zero voltage. Similarly, the D.C. offset in the current is related to the inductive nature of the compensator. These transient components can be considerably reduced by synchronizing the insertion of the filter in the following manner:

a) Close the first pole of the switch when the voltage across it is zero if the equivalent impedance, as seen from the terminals of this pole, is capacitive, or
b) Close the first pole of the switch when the voltage across it is at a peak if the equivalent impedance, as seen from the terminals of this pole, is inductive.
c) Follow the same criteria when closing the remaining poles except that correct account should now be made of the previously closed switch poles when the determining the Thevenin impedance.

The phase currents approach the post-fault steady state value by the end of the simulation period. This can be verified by comparing the plotted values with those in Table 4-2.

Instantaneous values of the current, at the fault terminals and through the high speed grounding switches at the sending and receiving terminals, are displayed in Fig.4-14. Restrictions in the compiled version of the EMTP used for this simulation precluded the use of a separate switch to emulate the fault function. As far as its correspondence with a real situation, the simulated fault would represent a fault located near the sending end grounding switch location. When interpreting the results, one should think of the current shown in Fig.4-14a as the superposition of that which flows through the faulted terminals and the grounding switch at the sending end. It corresponds to the fault current, from t=25 msec to t=70 msec, from fault inception to right after the grounding switch at the receiving terminal is closed and secondary arc current extinguished. The current through the high speed grounding switch at the sending end is shown from t=70 msec to the end of the simulation. It was assumed that high speed grounding of the faulted conductor at the remote terminals of the line is an effective method to squelch the secondary arc current. Modeling of the secondary arc current, and demonstrating the effectiveness of the high speed

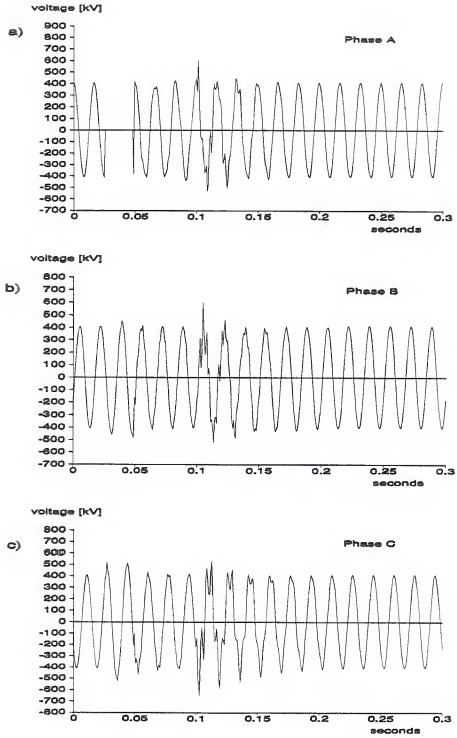

Fig.4-10. Instantaneous phase voltages at the sending terminal. a) Phase A, b) Phase B and c) Phase C.

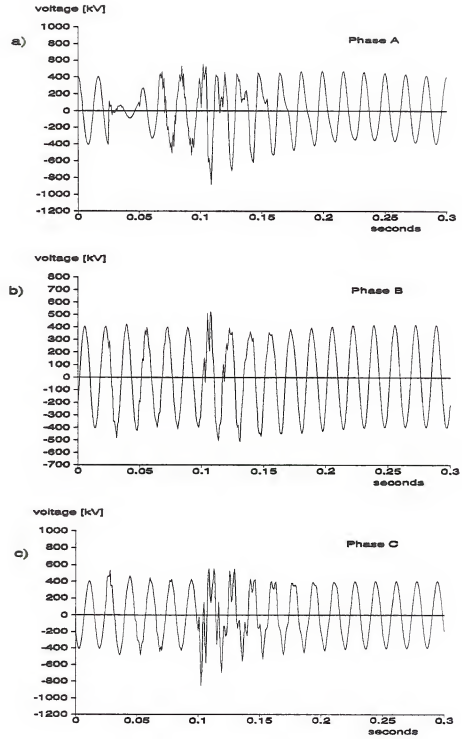

Fig.4-11. Instantaneous phase voltages at the receiving terminal. a) Phase A, b) Phase B and c) Phase C.

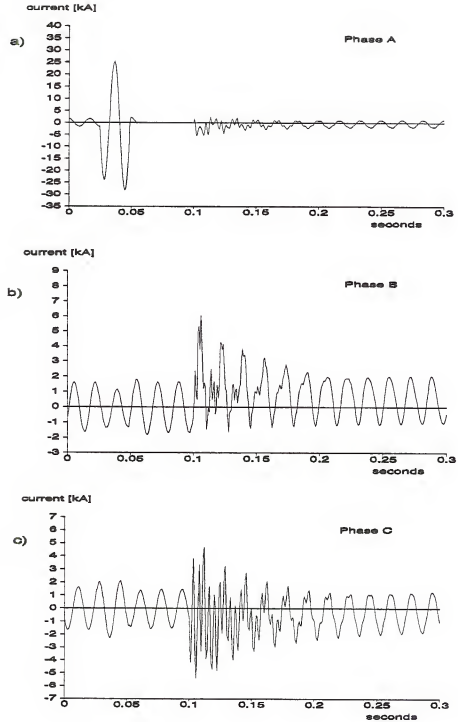

Fig.4-12. Instantaneous phase currents at the source side of the compensator in the sending end terminal. a) Phase A, b) Phase B and c) Phase C.

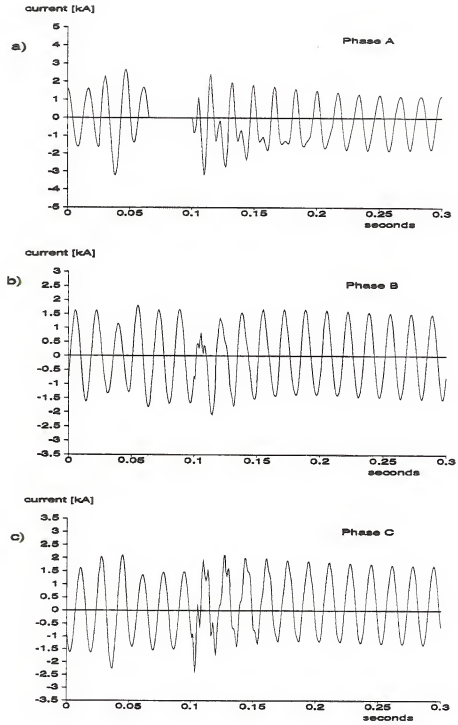

Fig.4-13. Instantaneous phase currents at the source side of the selective compensator in the receiving end terminal. a) Phase A, b) Phase B and c) Phase C.

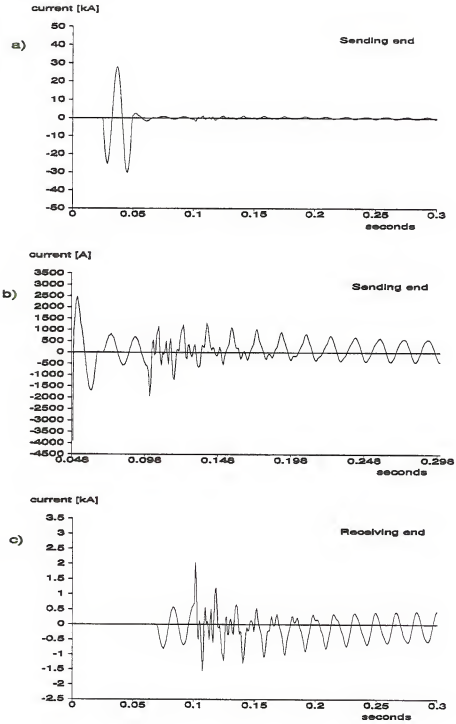

Fig.4-14. H.S.G.S Instantaneous currents at the sending end. a)complete simulation, b) after first breaker pole is opened and c) at the receiving end.

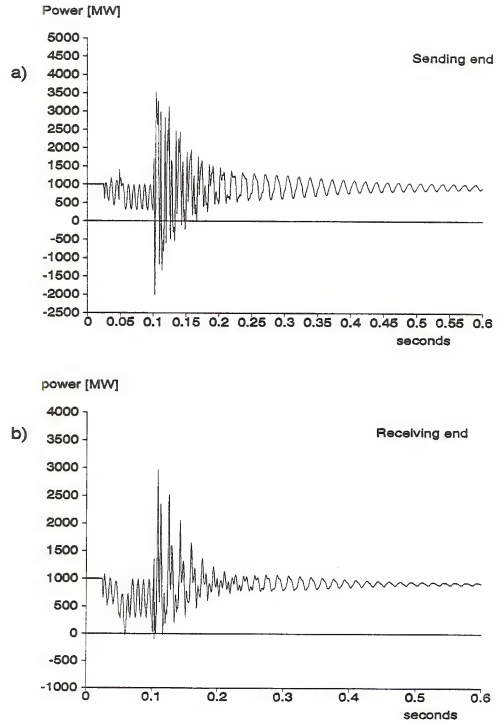

Fig.4-15. Instantaneous three phase power at source side of the selective sequence compensator. a) Sending and b) receiving terminals.

grounding switches in promoting its extinction lies outside the scope of this dissertation. These simulations are only intended to demonstrate the effectiveness of our compensating scheme under typical system configurations and proven operational practices. Secondary arc current modeling by EMTP, during SPO operations, has been previously documented by Goldberg et al. [14].

Figure 4-15 depicts the instantaneous three phase power at the sending and receiving end throughout the simulation period. The double frequency pulsating power, present during the time the fault is on and during unbalanced SPO operation, can be observed during part of the initial 100 msec of the simulation. Once the high frequency transients associated with the asynchronous insertion of the compensator have been attenuated, a high level of constant three phase power transfer is attained.

One Machine and Infinite Bus System

The final model used in this work to determine the effectiveness of our selective compensation scheme comprises a unit connected synchronous machine tie into an infinite system through a transmission line and an equivalent receiving source Thevenin equivalent. The sending end system of our base case is now replaced by a synchronous machine, modeled in the EMTP by a type-59 source component, and a step-up transformer in a delta grounded wye configuration to tap into the high

voltage system. The magnetizing current of the transformer and any saturation effects in the generator are neglected for simplicity. The equivalent one line diagram is shown in Fig.4-16.

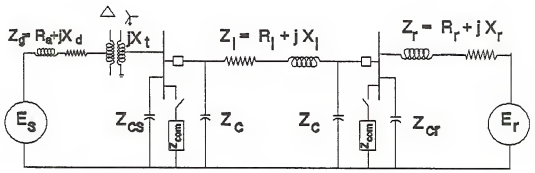

Fig.4-16. Single line diagram of one machine against infinite bus system.

System parameters, with the exception of those associated with the equivalent source impedance at the sending end, are as indicated in Table 3-1. Those associated with the sending end are shown in Table 4-3.

Table 4-3. One machine versus infinite bus system. Sending end impedances.

	Generator Impedance $Z_g = R_a + jX$ (p.u)*	Step-up Transformer Impedance Z_t (p.u)*
Positive Sequence	0.002655578 j 2.963342868 1)	0.00098631 j 0.06074366
Zero Sequence	0.002655578 j 0.18520893 2)	0.00098631 j 0.06074366

*) 100 MVA base. 1) $X = X_d$ 2) $X = X_0$

The remaining machine parameters correspond to those used in the EMTP benchmark case # DC-25 and are listed in appendix A.

The initial power transfer being received at the infinite system was fixed at 500 MVA at a power factor of 0.866 lagging. A one per unit voltage at an angle of 0° at the receiving bus was our defined reference voltage. The required dimensions of our compensator for the parameters and conditions specified are presented in Table 4-4.

To validate the steady state results generated by our program with those produced by the EMTP, under SPO and selective sequence compensation, the initial condition solution mode of the EMTP was run with the compensator permanently connected and the phase A poles of the line originally opened. The results from the EMTP were in agreement with ours only when the compensator was dimensioned based on the steady state equivalent positive sequence reactance of the machine, the X_d shown in Fig.4-16, replaced by its negative sequence reactance. This a consequence of the fact that in the steady-state and initial conditions solution mode, the EMTP sets the positive sequence impedance of the machine equal to its negative sequence impedance [15]. This is a requirement for obtaining a symmetric phase impedance matrix, an assumption made during network solution.

Table 4-4. Selective sequence compensator rating.
One machine and infinite system case.

Buses	A-G (MVAR)	B-G (MVAR)	C-G (MVAR)	A-B (MVAR)	B-C (MVAR)	C-A (MVAR)
Sending	-2.0	61	-59	-283	89.66	193.66
Receiving	23.66	-69	45.33	270	-72.33	-198.33
negative values = inductive VARS.						

Note that any impedance may be used in the positive sequence representation as long as the desired values for terminal voltage V_{pos} and current I_{pos} are obtained for the initial conditions; using the negative sequence impedance will produce a symmetric phase impedance matrix. Note that this simple machine model is used by the EMTP only in determining initial steady state conditions. A dynamic model describing the current flux-linkage relations of the rotor and stator coils and the electromechanical constraints of the machine is enabled during the time simulation period.

The dimension of the selective sequence compensator is presently determined based upon prescribed initial conditions of the system. The equivalent source voltages behind the Thevenin impedances used to represent the remote systems in our program, the synchronous machine and the infinite system, are assumed to remain constant in magnitude and angle

throughout the switching operations associated with SPO and compensator insertion. The open pole condition in conjunction with the sequence compensation produce a small increase in the effective transfer impedance between the equivalent sources. An aproximate expression used to determine the power transfer between the remote systems is given by (4-1) [16]

$$P_{transfer} \approx \frac{|E_s|\,|E_r|}{X_{eq}} \sin\delta \qquad (4\text{-}1)$$

X_{eq} is the equivalent positive sequence transfer impedance between the equivalent sources under the specified conditions and δ is the equivalent power angle, or difference between the sending and receiving source voltage angle.

Equation (4-1) clearly indicates that constant magnitude and angle equivalent source voltages subjected to an increase in equivalent transfer impedance between them result in a reduction in real power transfer. The EMTP logic assumes constant mechanical power into the machine as determined from the initial loading conditions of the modeled system. To simulate the required reduction in power input to the machine, associated with the SPO and compensation operation, it was necessary to make use of the Transient Analysis of Control Systems (T.A.C.S) feature of the EMTP. The TACS portion of the EMTP provides the required interface to simulate general control type arrangements. Output quantities from the network solution can be used as input quantities in TACS,

while output quantities from TACS can become input quantities to the network solution.

The case of one machine against an infinite system, corresponds to a generator synchronized to a network of such a large size that its frequency remains essentially constant, independent of the power output of this particular generator. For this configuration [17] there is a direct proportionality between the turbine power and the reference power setting, the change in frequency ($\Delta f_0 \approx 0$) playing a negligible part in determining the required turbine power.

$$\Delta P_{T,0} = \Delta P_{ref,0} - \frac{\Delta f_0}{R} \qquad (4\text{-}2)$$

where R is the generator droop or speed regulation constant.

To satisfy the requirements on the internal voltage of the machine it was necessary to simulate a step change, in the turbine power reference, during the SPO and compensation operation period. Not reducing the input power to the turbine during this period resulted in the machine lossing synchronism. Predetermining the optimum compensator values assuming constant input power to the machine, that is, allowing for the internal voltage angle to change, would have involved an iterative procedure. It is the author's opinion that simulating this last condition would not have provided additional information, in the evaluation of the feasibility of the proposed scheme, than that obtained by the current case.

The assumption of constant internal voltage magnitude, a requirement for the validity of the pre-determined compensator values, demanded a constant field voltage throughout the simulation thus obviating the need for excitation control.

The simple compensator model used in this work has proven effective for the case of strong sources interconnected by the affected line. Other applications in which one of the equivalent source voltages, and/or Thevenin source impedances varies during the compensation period, i.e. a machine connected to an infinite system, will require a continuously tunable or adaptive compensator. One whose components are dynamically adjusted based upon measurements of system unbalances. This new compensator model will permit evaluating interactions with the governor and excitation systems of a machine. This is the recommended next step in evaluating the effects of the selective sequence compensator in a power system.

The time sequence of events associated with this case is as follows:

t = 25 msec. Phase A pole opens at both the sending and receiving end terminals of the line.

t = 55 msec. Selective sequence compensator is switched in both sending and receiving buses.

t = 139 msec. Insertion resistors of the compensator are bypassed.

The steady state system operating values corresponding to the pre-opening and post-opening stages of the simulation are shown in Table 4-5. Figure 4-17 contains the plots of the instantaneous phase voltages at the terminals of the machine in the sending end. These are seen to stay within the required operational constraints. Instantaneous three phase power at the sending and receiving terminals of the line are shown in Fig.4-18. Once the switching transients have decayed, the instantaneous power approaches the value previously determined by our steady state solution and listed in Table 4-5, during SPO and selective compensation.

Figure 4-19a displays a plot of machine speed versus rotor angle. As the new operating point is approached it is seen that the variations in speed are reduced and the new rotor angle eventually attained. The small change in rotor angle is due to inaccuracies when determining the required change in the input power reference to the turbine according to our previous explanation. The exact solution would have shown the final angle approaching the original one.

The zero phase A current period between pole opening and compensator insertion is shown in Fig.4-20a. The high frequency transients and offset currents associated with the switching in of the compensator are present in all three phases.

Table 4-5. One machine - infinite system.
Initial conditions and post-fault steady state
under SPO and selective sequence compensation.

		Line terminal voltage [l-l,kV]	Equivalent source voltage [l-l,kV]	Phase current source side of compensator [A]	Real Power at line terminals [MW]	Reactive Power at line terminals [MVAR]
Sending end	initial	522.5 @ 4.9 (1.045 p.u)	43.34 @ 81.9 (1.759 p.u)	498.8 @ -10.1 (0.432 p.u)	436 (0.436 p.u)	120 (0.12 p.u)
	post-fault	522 @ 8.0 (1.044 p.u)	43.34 @ 81.9 (1.759 p.u)	481.5 @ -10.7 (0.417 p.u)	413 (0.413 p.u)	140 (0.14 p.u)
Receiving end	initial	500 @ 0 (1.0 p.u)	444.3 @ -13.2 (0.887 p.u)	577.3 @ -30 (0.5 p.u)	433 (0.433 p.u)	250 (0.25)
	post-fault	485. @ -2.3 (0.97 p.u)	444.3 @ -13.2 (0.887 p.u)	528.9 @ -24.2 (0.458 p.u)	406 (0.406 p.u)	179 (0.179 p.u)

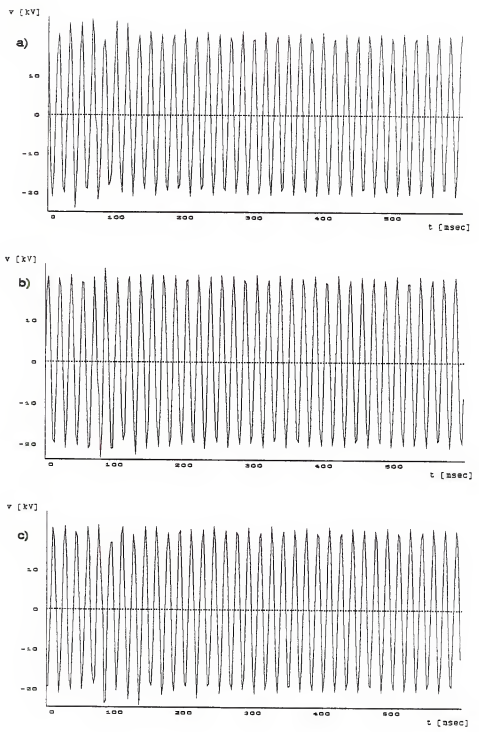

Fig.4-17. Instantaneous phase voltages at the machine terminals. Machine versus infinite system. a) Phase A, b) Phase B, and c) Phase C.

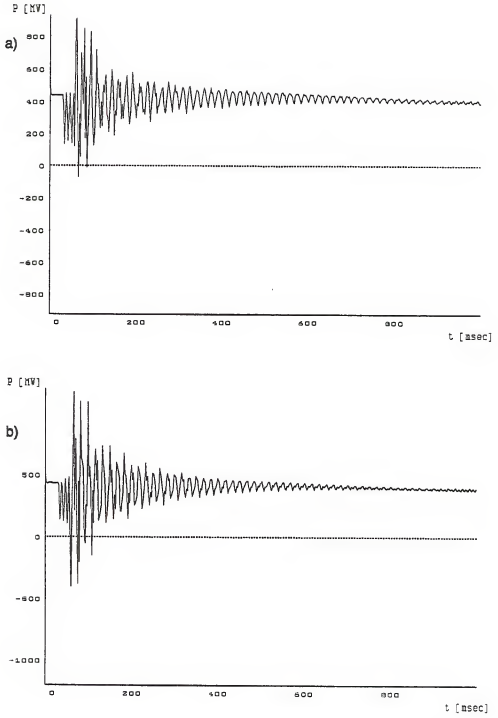

Fig.4-18. Instantaneous three phase power at the source side of the selective sequence compensator. a) Sending and b) receiving terminals.

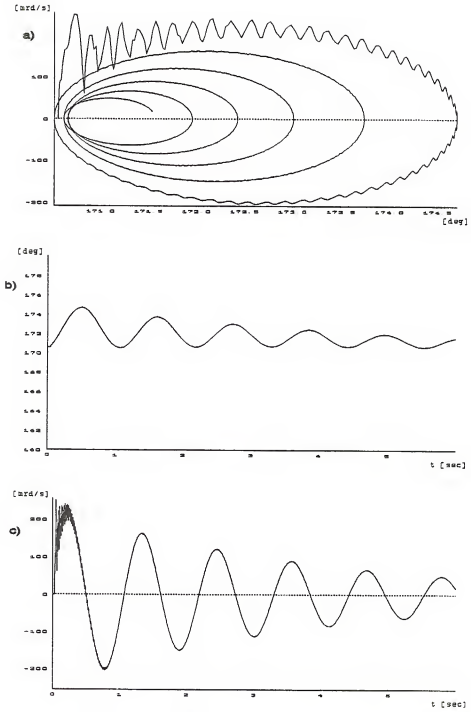

Fig.4-19. Mechanical variables for the machine versus infinite system case. a) Rotor speed deviation against machine power angle. b) Machine power angle and c) Rotor speed deviation from synchronous speed.

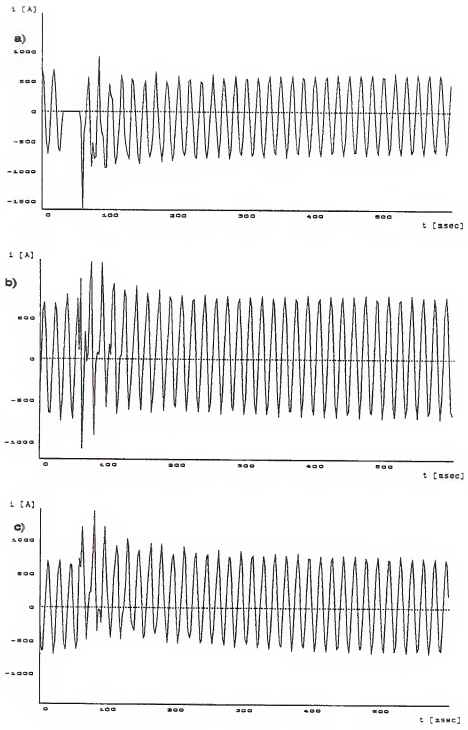

Fig.4-20. Instantaneous phase currents at the sending source side of the compensator. a) Phase A, b) Phase B, c) Phase C.

CHAPTER 5
CONCLUSIONS AND RECOMMENDATIONS

Conclusions

A new scheme or strategy that will allow three-phase A.C. transmission lines to be operated on a permanent basis, with one phase open, has been developed. Through the implementation of a new concept, selective sequence compensation, the undesired line sequence components of the current, generated during the single pole opening condition, are confined to flow in a restricted region of the system. Equal power transfer through the line, before and after the SPO condition, is obtained by shunt reactive compensation of the positive sequence network. Selective sequence compensation has made possible equivalent three phase power transfer in a two conductor circuit, thus simultaneously realizing a significant improvement in conductor utilization.

Operational constraints of the system, under steady state conditions, were satisfied for a wide range of system parameters variations under selective compensation. For the cases studied, the transient response of the system to the sudden insertion of our basic compensator, a switchable arrangement of fixed size passive reactive elements, was found

not to impose excessive duties on the related system components.

Even though the sizing of the compensator elements may appear somewhat larger than desired, the scheme, at this stage of development, may still prove appealing for lines serving emergency and high priority loads. It should be observed that for relatively low levels of power transfer, the sizing considerations of the compensator become less critical.

With the advent of new high power static switches, the synthesis of large reactive power generators with the use of smaller energy storage devices (capacitors and inductors), is becoming a more viable alternative [18,19,20]. Advancements in this area will certainly affect the feasibility of the proposed compensator, especially for transmission circuits used for transfering large amounts of power.

A by-product of this research has been the extension and development of a generalized method of analysis for multiple simultaneous faults of the parallel and series type, built upon transformations of the original bus impedance matrix.

Recommendations and Future Work

Additional work should be directed at developing a dynamic model for the sequence compensator. An adaptive version, adjustable in real time according to measurable instantaneous quantities (negative and zero sequence voltages

and currents) generated during loading conditions and system configurations.

Fast acting and time controlled solid state (i.e.,thyristors) switches can virtually eliminate high frequency transients and currents asymmetries normally associated with compensator insertion. The increase in switching speed will improve the transient stability margin of the system, for phase to ground faults, by shortening the time during which the line is operated at an increased value of transfer impedance while operating under SPO and no compensation.

Interactions of this proposed compensator model with excitation and automatic generation control systems should now be adressed without the restrictions, in the time simulation (EMTP) of the compensation sequence, imposed by the constraint of constant equivalent source voltages, inherent in the original model.

The determination of the feasibility of a series connected compensator, as a complement or substitute to the one presented in this dissertation should also be given serious consideration. A series selective sequence compensator would ideally be designed to impede the flow of selected sequence components of the current at its location.

Compensation of the zero sequence reactance of the line, to guarantee high levels of power transfer during SPO conditions deserves careful investigation.

The application of selective sequence compensation can be extended to less conventional operating conditions. Safe operation of a three phase circuit with only one conductor (with ground return) in service is theoretically possible by suitable sequence compensation. As a consequence, only faults involving all three phases, a rare ocurrence, would require complete circuit isolation.

APPENDIX A
SYNCHRONOUS MACHINE DATA

The machine parameter data, used in the simulation of the Type-59 dynamic synchronous machine source component model, was obtained from the EMTP benchmark case # DC-25. Table A-1 contains the corresponding values.

Table A-1. Machine parameters.

KV	MVA	Ra	Xl	Xd	Xq	X'd	X'q
26	722	0.00172	0.19	1.92	1.85	0.31	0.6
X''d	X''q	T'do	T'qo	T''do	T''qo	Xo	Rn
0.26	0.26	4.8	1.0	0.04	0.053	0.12	1.E-6
Xn	WR^2	DSR					
1.E-6	0.87	1.E-3					

where the symbols correspond to

KV : Rated or base machine voltage (kilovolts).

MVA : Rated or base three phase rated volt-ampere rating of machine. (var X 10^6)

WR^2 : Moment of Inertia of rotor mass (10^6 pound-$feet^2$)

DSR : Speed deviation self damping coefficient (pound-$feet^2$*sec/rad)

Machine resistance and reactances in per unit of machine base

Ra : Armature resistance.

Xl : Armature leakage reactance.

Xd : Direct-axis synchronous reactance.

X'd : Direct-axis transient reactance.

X'q : Quadrature-axis transient reactance.

X"d : Direct-axis subtransient reactance.

X"q : Quadrature-axis subtransient reactance.

Xo : Zero sequence reactance.

Rn : Real part of the neutral grounding impedance.

Xn : Imaginary part of neutral grounding impedance.

Machine time constants in seconds

T'do : Direct-axis open-circuit transient time constant.

T'qo : Quadrature-axis open-circuit transient time constant.

T"do : Direct-axis open-circuit subtransient time constant.

T"qo : Quadrature-axis open-circuit subtransient time constant.

The data corresponding to the generator step-up transformer, shown in Fig.4-16, is presented in Table A-2.

Table A-2. Step-up transformer data.

winding	R	Xl
delta	0.00071	0.04368
grounded Y	0.149045	9.185621

kV : Rated line to line voltage of transformer winding, in kilovolts.

R : Winding resistance in ohms. At same winding voltage base.

Xl : Winding leakage reactance in ohms. (idem)

APPENDIX B

EMTP DATA FILE LISTING

The EMTP data file, used for simulating the synchronous machine against an infinite system case, is listed next.

```
RELATIVE TACS DIMENSIONS
      1       1       1      12       2      60       1      22
BEGIN NEW DATA CASE
$CLOSE, UNIT=4 STATUS=DELETE
$OPEN, UNIT=4 FILE=DUMMY.PL4 FORM=UNFORMATTED STATUS=UNKNOWN
C  filename:emtpdis.dat
C  Interconnected synchronous machine (type SM-59) and infinite system
C  (ideal voltage source) by a lumped resistor, frequency independent
C  distributed parameter transmission line.
C  Simulates SPO phase A and preinsertion  resistor switching
C  (w/o synchronizing). Also looks at machine transients during switching
C  compensator period. Prefault load: 500 MW.
C  Uses subtransient reactance for -ve seq. of generator and synchronous
C  reactance for its +ve sequence when computing filter parameters.
C  MISCELLANEOUS DATA CARDS.
C 345678901234567890123456789012345678901234567890123456789012345678901234567890
   2.E-4  6.0E-0    60.0    60.0
     100      10       1       1                                      2
C
C
TACS HYBRID               COMPUTES TOTAL 3-PHASE POWER AT SENDING & REC. ENDS.
C 345678901234567890123456789012345678901234567890123456789012345678901234567890
90VSAT                 60.0                                          -1.
90VSBT                 60.0                                          -1.
90VSCT                 60.0                                          -1.
90VRAT                 60.0                                          -1.
90VRBT                 60.0                                          -1.
90VRCT                 60.0                                          -1.
91VSATX                60.0                                          -1.
91VSBTX                60.0                                          -1.
91VSCTX                60.0                                          -1.
91VRATX                60.0                                          -1.
91VRBTX                60.0                                          -1.
91VRCTX                60.0                                          -1.
C 345678901234567890123456789012345678901234567890123456789012345678901234567890
88PTINI    =507.08
11TEST     -0.05275                                          0.06
98MEPOW    =1.0*TEST
99PSA      =VSAT*VSATX
99PSB      =VSBT*VSBTX
99PSC      =VSCT*VSCTX99PRA      =VRAT*VRATX
99PRB      =VRBT*VRBTX
99PRC      =VRCT*VRCTX
99PST      =PSA+PSB+PSC
99PRT      =PRA+PRB+PRC
C   TACS PRINTED/PLOTTED OUTPUT.
33PST   PRT   MEPOW SPEED DELPT DELPTUVFIEL
C INITIAL CONDITIONS
```

```
77PST     .50506E+09
77PRT     .49599E+09
77MEPOW   1.0
BLANK CARD ENDING TACS SIMULATION
C  BRANCH CARDS.
$VINTAGE, 1
C DISTRIBUTED PARAMETER-FREQ INDEPENDENT LUMP RESISTIVE  MODEL FOR A TRANSPOSED
C TRANSMISSION LINE. ---SEE SECTION 7.3.2 OF EMTP MANUAL.
C 34567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
-1VSAL  VRAL                5089.E-02   16606.E-2 5347594.E-4          1.0 0 0
-2VSBL  VRBL                3635.E-03   52965.E-3   68228.E-2          1.0 0 0
-3VSCL  VRCL
$VINTAGE, 0
$VINTAGE, 1
C
C FILTER PARAMETERS.[Reactive Compensator].
C SENDING END.
C 34567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
C *BUS1*-BUS2-              *******R**********------WL--------********WC********
C     LINE IMPEDANCE CHANGE.
C
 0VSCOM                     0.000001
 0VSATY VSATYY              5.00
 0VSBTY VSBTYY              5.00
 0VSCTY VSCTYY              5.00
 0VSATY VSTYCO              46134.E-2       46134.E+0
 0VSBTY VSTYCO                0.1                            66960.E-2
 0VSCTY VSTYCO              15442.E-3       15442.E-1
 0VSTYCO                 0.000001
 0VSATY VSBTY               96302.E-4       96302.E-2
 0VSATY VSCTY                 0.1                          71000.E-2
 0VSBTY VSCTY                 0.1                          32824.E-2
C RECEIVING END.
 0VRATY VRATYY              5.00
 0VRBTY VRBTYY              5.00
 0VRCTY VRCTYY              5.00
 0VRATY VRTYCO                0.1                          30052.E-2
 0VRBTY VRTYCO              11348.E-3       11348.E-1
 0VRCTY VRTYCO                0.1                          58080.E-2
 0VRTYCO                 0.000001
 0VRATY VRBTY                 0.1                          11516.E-1
 0VRATY VRCTY               11843.E-3       11843.E-1
 0VRBTY VRCTY               32531.E-3       32531.E-1
C
$VINTAGE,0
C    SENDING AND RECEIVING BUS CAPACITANCES. (Zcs,Zcr).
$VINTAGE,1
 1VSATX                             1.E20                    4071695.E-4
 2VSBTX                                                      -702514.E-4
                                    1.E20                    4071695.E-4
 3VSCTX                                                      -702514.E-4
                                                             -702514.E-4
                                    1.E20                    4071695.E-4
 1VRATX                             1.E20                    1176027.E-4
 2VRBTX                                                      -188013.E-4
                                    1.E20                    1176027.E-4
 3VRCTX                                                      -188013.E-4
                                                             -188013.E-4
                                    1.E20                    1176027.E-4
$VINTAGE,0
C 34567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
C    EQUIVALENT SOURCE IMPEDANCE AT RECEIVING END.
51VRA   VRATX           27.40   10837.50E-2
52VRB   VRBTX           4.08    11952.50E-2
53VRC   VRCTX
C
```

```
C  STEP-UP TRANSFORMER
C
C 3456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
  TRANSFORMER                          TRAN A
          9999
 1VSA    VSC              .00071.0436824.63
 2VSATX VSCOM             .149049.1856288.7
  TRANSFORMER TRAN A                   TRAN B
 1VSB    VSA
 2VSBTX VSCOM
  TRANSFORMER TRAN A                   TRAN C
 1VSC    VSB
 2VSCTX VSCOM
$VINTAGE,1
C   Capacitance to ground in delta corners of transformer.(to provide connection
C   to ground in delta side). Value, typical of xmer (0.003uf).
C   See page 4E-7 of ATP manual.
  0VSA                                                                .1131E+1
  0VSB                                                                .1131E+1
  0VSC                                                                .1131E+1
$VINTAGE,0
BLANK CARD ENDING BRANCH CARDS.
C 3456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
C ---------------SENDING AND RECEIVING INTERRUPTING SWITCHES--------------
  VSAT  VSAL    -1.E+0    25.E-3      0.0
  VSBT  VSBL    -1.E+0     1.E+3      0.0
  VSCT  VSCL    -1.E+0     1.E+3      0.0
  VRAL  VRAT    -1.E+0    25.E-3      0.0
  VRBL  VRBT    -1.E+0     1.E+5      0.0
  VRCL  VRCT    -1.E+0     1.E+5      0.0
C ---------------------LINE METERING SWITCHES-----------------------------
  VSATX VSAT                                              MEASURING
  VSBTX VSBT                                              MEASURING
  VSCTX VSCT                                              MEASURING
  VRAT  VRATX                                             MEASURING
  VRBT  VRBTX                                             MEASURING
  VRCT  VRCTX                                             MEASURING
C ------------------------ FILTER SWITCHES -----------------------------
C 3456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
  VSAT  VSATYY 55.E-3     1.E+5      0.0
  VSBT  VSBTYY 55.E-3     1.E+5      0.0
  VSCT  VSCTYY 55.E-3     1.E+5      0.0
  VRAT  VRATYY 55.E-3     1.E+5      0.0
  VRBT  VRBTYY 55.E-3     1.E+5      0.0
  VRCT  VRCTYY 55.E-3     1.E+5      0.0
C ------------------------INSERTION SWITCHES-------------------------------
  VSATYYVSATY 139.E-3     1.E+5      0.0
  VSBTYYVSBTY 139.E-3     1.E+5      0.0
  VSCTYYVSCTY 139.E-3     1.E+5      0.0
  VRATYYVRATY 139.E-3     1.E+5      0.0
  VRBTYYVRBTY 139.E-3     1.E+5      0.0
  VRCTYYVRCTY 139.E-3     1.E+5      0.0
BLANK CARD ENDING SWITCH CARDS
C 3456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
C     //Ampl+.//----Hz.----''deg''''**A1*******              *Tstart***
14VRA     1.3627980E6 60.0      -13.182    0.0                 -1.0
14VRB     1.3627980E6 60.0      226.818    0.0                 -1.0
14VRC     1.3627980E6 60.0      106.818    0.0                 -1.0
C BUS       |VOLT|   FREQ      ANGLE
C         L-n,Pk
59VSA      21090.     60.0      36.29
  VSB
  VSC
TOLERANCES                                                  20
PARAMETER FITTING       2.0
C 3456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
 1 1      21.         1.          722.      26.        1.31061E+4
BLANK card for the Q-axis
```

```
.001720594.19       1.92       1.85      .31       0.6       .26       .26
4.8         1.0       .04       .053      .12       .000001   .000001
 1          1.0        .87       .001
BLANK card ending mass cards
C 3456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
  11
  52
  21
  31
BLANK card ending output specifications for this S.M.
C   TACS-MACHINE INTERFASE VARIABLES.
C 3456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
72MEPOW          1
  FINISH
BLANK CARD ENDING SOURCE CARDS
C  NODES FOR PLOTTING
C 3456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
  VSA    VSB    VSC    VSAL   VSBL   VSCL
C VSAT   VSATY VSBT   VSBTY VSCT   VSCTY
BLANK CARD ENDING SELECTIVE NODE VOLTAGE OUTPUTS
 2 PLOT OF SWITCH VOLTAGE & CURRENTS.
C 3456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
 1943.0 0.0 10.          VSAT   VSAL   VSBT   VSBL
BLANK CARD ENDING PLOT CARDS
BEGIN NEW DATA CASE
BLANK CARD
```

REFERENCES

[1] Edward W. Kimbark, "Suppresion of Ground-Fault Arcs on Single Pole Switched EHV Lines by Shunt Reactors", IEEE Trans., March 1964, pp. 285-290.

[2] B.R.Shperling, A.Fakheri, "Compensation Scheme for Single Pole Switching on Untransposed Transmission Lines", IEEE Trans., July/August 1978, PAS-97, pp. 1421-1429.

[3] B.R.Shperling, A.Fakheri, "Single Phase Switching Parameters for Untransposed EHV Lines", IEEE Trans., March/April 1979, PAS-98, pp. 643-654.

[4] R.M.Hasibar, A.C.Legate, J.Brunke, W.G.Peterson, "The Application of High Speed Grounding Switches for Single Pole Reclosing on 500 KV Power Systems", IEEE Trans., April 1981, PAS-100, pp. 1512-1515.

[5] B.Shipley, H.J.Holley, D.W.Coleman, "Digital Analysis of Single-Pole Switching on EHV LInes", IEEE Trans., August 1968, PAS-87, pp. 1679-1687.

[6] Z.X.Han, "Generalized Method of Analysis of Simultaneous Faults in Electric Power Systems", IEEE Trans., October 1982, PAS-101, pp. 3933-3942.

[7] M.S.Sachdev, R.Agarwal, "A Technique for Estimating Transmission Line Fault Locations from Digital Impedance Relay Measurements", IEEE Trans., January 1988, PD-3, pp. 121-129.

[8] W.S.Meyer and T.H.Liu, Eds., "EMTP Rule Book", Portland, Oregon: Bonneville Power Administration, System Engineering, June,1984.

[9] L.Gyugy, R.A.Otto, T.H.Putman, "Principles and Applications of Static Thyristor-controlled Shunt Compensators", IEEE Trans., 1978, PAS-97, pp. 1935-1945.

[10] ANSI C37-06-1979, "Preferred Ratings and Related Required Capabilities for AC High Voltage Circuit Breakers Rated on a Symmetrical Current Basis".

[11] R.W.Alexander, "Synchronous Closing Control for Shunt Capacitors", IEEE Trans., 1985, PAS-105, pp. 2612-2626.

[12] Thomas E. Browne, Jr., ed. "Circuit Interruption, Theory and Techniques", Marcel Dekker, Inc., New York, 1984.

[13] Allan Greenwood, "Electrical Transients in Power Systems", Wiley-Interscience, New York 1976.

[14] Saul Goldberg, W.F.Horton, D.Tziouvaras, "A Computer Model of the Secondary Arc in Single Phase Operation of Transmission Lines" IEEE Trans., 1989, PD-4, pp. 586-595.

[15] H.W.Dommel, "EMTP Theory Book", Portland, Oregon: Bonneville Power Administration, April 1987.

[16] Olle Elgerd, "Basic Electric Power Engineering", Addison-Wesley, Philippines 1977.

[17] P.M.Anderson, A.A.Fouad, "Power System Control and Stability", The Iowa State University Press, 1977.

[18] Olle Elegerd, "Electric Energy Systems Theory, an Introduction", McGraw-Hill Co, New York 1982.

[19] H.Akagi, Y.Kanazawa, A.Nabae, "Instantaneous Reactive Power Compensators Comprising Switching Devices without Energy Storage Components", IEEE Trans., 1984, IA-20, pp. 625-630.

[20] L.Gyugyi, F.Cibulka, "The High Frequency Base Converter. A New Approach to Static High Power Conversion", IEEE Trans., 1979, IA-15, pp. 420-429.

[21] L.Gyugyi, "Reactive Power Generation and Control by Thyristor Circuits", IEEE Trans., 1979, IA-15, pp. 521-532.

BIOGRAPHICAL SKETCH

Orlando A. Ciniglio was born in Panama, Republic of Panama, on October 25, 1955. He received his B.S.E.E. from Louisiana State University in 1976 and his M.S.E.E. degree from Texas A & M University in 1977. He began his engineering carrer with I.R.H.E., the national power company in Panama, where he advanced to the position of Chief Protection Engineer. Mr. Ciniglio is presently working in the System Protection Department of Idaho Power Company.

I certify that I have read this study and that in my opinion it conforms to acceptable standard of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Dennis P. Carroll, Chairman
Professor of Electrical
Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standard of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Jacob Hammer, Cochairman
Associate Professor of
Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standard of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Alexander Domijan
Assistant Professor of
Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standard of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Murali Rao
Professor of Mathematics

I certify that I have read this study and that in my opinion it conforms to acceptable standard of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Khai Ngo
Assistant Professor of
Electrical Engineering

This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

May 1991

for Winfred M. Phillips
Dean, College of Engineering

Madelyn M. Lockhart
Dean, Graduate School